DOCKET NO.: 217208US- 8

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF		:
HARUO FURUTA ET AL		: EXAMINER: OWENS, D.
SERIAL NO: 10/014,345		:
FILED: DECEMBER 14, 2001		: GROUP ART UNIT: 2811
FOR:	SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREFOR	:

PETITION UNDER 37 C.F.R. § 1.182

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Applicants in the above-identified patent application hereby petition the Commissioner of the U.S. Patent and Trademark Office (hereinafter "the Office") to replace the specification, claims and drawings in the Office's file for the above-identified application, with the copy of the specification, claims and formal drawings that were actually filed in this application, and attached hereto as Appendix A.

BACKGROUND

Applicants first discovered that the Office was examining a different patent application than the one filed in this case when the undersigned received an Office Action dated September 9, 2002, containing a Restriction Requirement indicating that Claims 1-10 are subject to restriction and/or election requirement, while the filed application included 13 claims. Upon noticing this discrepancy, Applicants filed a "Power to Inspect and To Make Copies" so as to obtain a photocopy of the application in the Office's file. Upon looking at

the first page of the specification (see Appendix B) in the Office's file, it became clear that the Office had mistakenly entered a "related pending application" that Applicants attached to a Related Case Statement, consistent with Rule 56. The front page of the specification in the Office's file bears a stamp "Related Pending Application" used by the undersigned's law firm to identify related pending applications. This stamp indicates that the application is a related pending application and includes a serial number and filing date for that related pending application.

EVIDENCE SUPPORTING THE REPLACEMENT OF THE PATENT APPLICATION OF APPENDIX A FOR THE APPLICATION IN THE OFFICE'S FILE

Appendix C is a date-stamped filing receipt that bears the December 14, 2001 stamp from the Office, and indicates that the specification, drawings and claims of Appendix A was actually filed on December 14, 2001. As can be seen, the date-stamped filing receipt indicates that the Office received on December 14, 2001 a specification having 36 pages, 13 claims and 18 drawing sheets. The date-stamped filing receipt bears the attorney docket number of 217208US-2. Appendix A, copied from Applicants' file, does in fact include exactly 36 pages, while the specification included in the Office's file includes 48 pages. The date-stamped filing receipt of Appendix C indicates that 13 claims were filed, which is exactly the same as the number of claims from Applicants' file, while the Office's copy includes 10 claims. The date-stamped filing receipt indicates that 18 drawing sheets were filed, which is exactly the same as the number of drawing sheets from Applicants' file, and coincidently the Office's copy also indicates18 drawing sheets are included in specification in the Office's file. The drawings found in the Office's copy include the attorney docket number 217208US2, and are identical to those drawings contained in Applicants' file. The date-stamped filing receipt of Appendix C also indicates that an Information Disclosure Statements/List of Related Cases was filed along with one cited pending application. The

undersigned expects that the Office must have mistakenly considered this one cited pending application as the filed application instead of the application of Appendix A. As further evidence of this mistaken substitution, the date-stamped filing receipt indicates that a cited pending application was filed with the application, but no cited pending application was found in the Office's file when our searcher returned with a complete file wrapper copy the entire Office's file.

Applicants' file does include an Information Disclosure Statement, that includes a List of Related Cases, (Appendix D) which identifies the related case as our client reference MD-691 (513823), having serial number 09/340,504, and no filing date. This client reference number and serial number are all included on page 1 of the specification included in the Office's file, which Applicants intended (and appropriately marked) so as to not be confused for the case to be examined.

Attached hereto as Appendix E is a Declaration of Arlene Huff, Assistant Supervisor, who confirms that the specification, claims and drawings of Appendix A, are in fact a copy of the specification, drawings and claims of Applicants' file and have remained unchanged since the December 14, 2001 filing.

The Office's copy of the Utility Patent Application Transmittal includes a USPTO barcode, identifying the serial number as 10/014,345, which means that the Office associated the assigned serial number 10/014,345 with the cover pages for the application identified in Appendix A, which includes Attorney Docket Number 217208US2, as noted at the top of the Utility Patent Application Transmittal Form in Appendix F, but not the correct specification.

Lastly, as identified in Appendix G, the Fee Transmittal Form, that bears docket number 217208US2, indicates that 13 total claims have been paid for, not the 10 claims that are included in the related application, mistakenly included as the application to be examined by the Office.

CONCLUSION AND REQUEST FOR RELIEF

In view of the evidence presented above, it appears as though the Office has mistakenly substituted a "cited pending application" for the application that Applicants filed on December 14, 2001. Because the present specification, drawings, and claims (Appendix A) were filed with a cited pending application (as part of a Related Case Statement), it is quite possible that the Office mistakenly entered the cited pending application as the filed application.

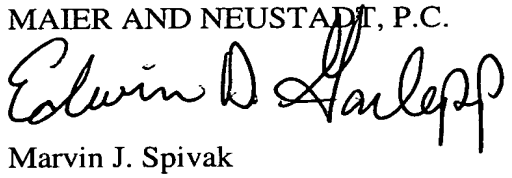
Consequently, Applicants respectfully request that the specification, claims and drawings of Appendix A, be substituted for the specification, claims and drawings that is presently included in the Office's file and was the subject of the Restriction Requirement in the Office Action of September 9, 2002. Furthermore, after the grant of this Petition, Applicants request a new Office Action, based on the specification, claims and drawings of Appendix A.

The fee as required under §1.17(i) for the present petition of **$130.00** is enclosed. In the event any variance exists between the amount enclosed and the Patent Office charges for filing the above-noted documents, including any fees required under 37 CFR 1.136 for any necessary Extension of Time to make the filing of the attached documents timely, please charge or credit the difference to our Deposit Account No. 15-0030. Further, if these papers

are not considered timely filed, then a petition is hereby made under 37 C.F.R. 1.136 for the necessary extension of time. A duplicate of this sheet is enclosed.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER AND NEUSTADT, P.C.



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TITLE OF THE INVENTION

Semiconductor Device and Manufacturing Method Therefor

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a semiconductor device and a method of manufacturing the semiconductor device, especially to MOS transistors with gate insulating films of different thickness and a method of manufacturing such MOS transistors.

Description of the Background Art

For cost reduction and performance improvement over semiconductor devices, it is essential to scale down the semiconductor devices. For the scale-downs, a gate insulating film of each MOS transistor needs to be as thin in thickness as the other parts of the transistor. The reduction of the thickness of the gate insulating film, however, causes a reduction in the gate breakdown voltage of the MOS transistor.

While the MOS transistor with a thin gate insulating film is suitable as transistors which make for example a logic circuit for performing a logic operation (the breakdown voltage of which is 2-5 V), it is not suitable for circuit portions such as an input circuit which require a relatively high breakdown voltage (5-10 V).

In recent semiconductor integrated circuit devices which comprise on the same substrate circuit portions operating at different driving voltages (e.g., a logic circuit, an input/output circuit, a memory portion), a plurality of kinds of MOS transistors with gate insulating films of different thickness are properly used depending on the circuit portions, whereby the scale-downs of the semiconductor devices are achieved.

For example, a region where a MOS transistor having a 1- to 4-nm-thick gate

insulating film and operating at a driving voltage of 0.8 to 1.8 V is located, is referred to as a "thin-film portion", while a region where a MOS transistor having a 4- to 12-nm-thick gate insulating film and operating at a driving voltage of 1.8 to 5 V is located, is referred to as a "thick-film portion". And each portion is formed of a proper MOS transistor.

Such a technique of using gate insulating films (especially, gate oxide films) of different thickness is called a dual oxide process and is getting important these days.

Referring now to Figs. 28 and 29, two kinds of MOS transistors 10 and 20 formed by a conventional dual oxide process will be described hereinbelow.

Fig. 28 shows cross-sectional shapes of the MOS transistors 10 and 20 longitudinally of their gates, and Fig. 29 shows cross-sectional shapes thereof transversely of the gates.

As shown in Figs. 28 and 29, the MOS transistor 10 is formed with a relatively thick gate oxide film in a thick-film portion AR, and the MOS transistor 20 is formed with a relatively thin gate oxide film in a thin-film portion BR.

The MOS transistors 10 and 20 are located in active regions 3A and 3B, respectively, which are defined by an isolation insulating film 2 formed in the surface of a semiconductor substrate 1. The isolation insulating film 2 is a kind of element isolation insulating films called STI (Shallow Trench Isolation).

In the surfaces of the active regions 3A and 3B, well regions 4A and 4B are located, respectively, and channel implant regions 5A and 5B are located in the surfaces of the well regions 4A and 4B, respectively.

On the main surface of the semiconductor substrate 1, gate oxide films GX1 and GX2 of different thickness are located in the active regions 3A and 3B, respectively, and gate electrodes GT1 and GT2 are located on top of the gate oxide films GX1 and

GX2, respectively.

Further, an interlayer insulation film 6 is located to cover the gate electrodes GT1 and GT2, on top of which planarized interlayer insulation films 7 and 8 are located.

Corresponding to the MOS transistors 10 and 20, contact portions 9A and 9B are provided, respectively, passing through the interlayer insulation films 6 to 8. As shown in Fig. 29, the contact portions 9A and 9B are electrically connected to source/drain regions SDA and SDB of the MOS transistors 10 and 20, respectively. Further as shown, sidewall oxide films GW1 and GW2 are located on the side faces of the gate electrodes GT1 and GT2, respectively.

The gate electrodes GT1 and GT2 are also connected respectively to the contact portions 9A and 9B, which is however not shown in Figs. 28 and 29 for convenience's sake.

As shown in Figs. 28 and 29, the isolation insulating film 2 which defines the active region 3B in the thin-film portion BR has an excessively removed edge portion on the side of the MOS transistor 20, and thereby a recess is formed in the edge portion of the active region 3B.

Next, a method of manufacturing the MOS transistors 10 and 20 will be described step by step with reference to Figs. 30 to 34.

In a step of Fig. 30, the isolation insulating film 2 is selectively formed in the surface of the semiconductor substrate 1 to define the active regions 3A and 3B. After formation of a thermal oxide film (not shown), the well regions 4A, 4B and the channel implant regions 5A and 5B are formed by impurity ion implantation, more specifically well formation and channel doping, in the active regions 3A and 3B.

In a step of Fig. 31, the main surfaces of the active regions 3A and 3B are thermally oxidized to form an oxide film OX3 of a third thickness. Here, the "third

thickness" is defined as a resultant thickness from subtraction of a second thickness from a first thickness, where the first and second thicknesses are respectively the thicknesses of the gate oxide films GX1 and GX2 to be formed later.

In a step of Fig. 32, a resist pattern RM1 is formed by a photolithographic technique to cover the thick-film portion AR.

Then, the oxide film OX3 in the thin-film portion BR is removed by wet etching for a predetermined period of time. At this time, the edge portion of the isolation insulating film 2 formed of an oxide film is excessively removed and thereby the active region 3B is protruded.

After removal of the resist pattern RM1, in a step of Fig. 33, the oxide film OX3 is increased in thickness to form the gate oxide film GX1 of the first thickness on top of the active region 3A. At this time, the gate oxide film GX2 of the second thickness is formed on top of the active region 3B.

In a step of Fig. 34, a conducting layer CL is formed to cover the gate oxide films GX1 and GX2.

The conducting layer CL is patterned to form the gate electrodes GT1 and GT2. With the gate electrodes GT1 and GT2 as masks, ion implantation is carried out to form the source/drain regions SDA and SDB in the active regions 3A and 3B, respectively.

After the interlayer insulation films 6 to 8 are stacked one above the other over the whole surface, the contact portions 9A and 9B are formed, reaching the source/drain regions SDA and SDB respectively through the interlayer insulation films 6 to 8. This provides the MOS transistors 10 and 20 shown in Figs. 28 and 29.

In the conventional dual oxide process, as has been described, the oxide film OX3 is once formed and then removed by wet etching to form the thin gate oxide film GX2 in the thin-film portion BR. The edge portion of the isolation insulating film 2 is

thus excessively removed and thereby the active region 3B is protruded.

Fig. 35 shows the details of a region X in Fig. 33. As shown in Fig. 35, a depth of an excessively removed portion of the edge portion of the isolation insulating film 2 which faces the active region 3B is 5 nm (50 Å) or less, the depth being defined as a depth between the main surface of the active region 3B and the deepest part of the recess. The horizontal distance between the active region 3B and the isolation insulating film 2 is 0. 1 μm or less and the angle of inclination of the protruded portion of the active region 3B ranges from 65° to 90°.

Such an excessively removed portion of the edge portion of the isolation insulating film 2 causes a reduction in threshold voltage due to an inverse narrow-channel effect. Further, the depth of an excessively removed portion varies depending on the time for wet etching of the oxide film OX3 in the thin-film portion BR.

Consequently, the threshold voltage varies depending on the depth of an excessively removed portion of the edge portion of the isolation insulating film 2, which considerably reduces manufacturing yield of the semiconductor device.

SUMMARY OF THE INVENTION

A first aspect of the present invention is directed to a semiconductor device comprising: a semiconductor substrate; an isolation insulating film selectively located in a surface of the semiconductor substrate; and first and second transistors located respectively on first and second active regions which are defined by the isolation insulating film. The first transistor has a first gate insulating film of a first thickness which is selectively located on the first active region, and the second transistor has a second gate insulating film of a second thickness which is selectively located on the second active region. The first thickness is greater than the second thickness. The

isolation insulating film has a recessed portion in an edge portion on the side of either the first or second active region, the recessed portion being located around either the first or second active region. A depth of the recessed portion is defined as a depth at which threshold voltage of either the first or second transistor is substantially constant according to a characteristic of variation in threshold voltage of either the first or second transistor with respect to variation in depth of the recessed portion.

According to a second aspect of the present invention, the depth at which threshold voltage of either the first or second transistor is substantially constant is a depth at which a range of variation in threshold voltage of either the first or second transistor is 5 to 10% of a maximum range of variation according to the characteristic of variation.

According to a third aspect of the present invention, the depth of the recessed portion is defined as a vertical height between a main surface of the first active region and a deepest part of the recessed portion, and is not less than 10 nm.

A fourth aspect of the present invention is directed to a semiconductor device comprising: a semiconductor substrate; an isolation insulating film selectively located in a surface of the semiconductor substrate; and first and second transistors located respectively on first and second active regions which are defined by the isolation insulating film, the first transistor having a first gate insulating film of a first thickness which is selectively located on the first active region, the second transistor having a second gate insulating film of a second thickness which is selectively located on the second active region, the first thickness being greater than the second thickness, the isolation insulating film having a recessed portion in an edge portion on the side of the first active region, the recessed portion being located around the first active region.

According to a fifth aspect of the present invention, the depth of the recessed portion is defined as a vertical height between a main surface of the first active region and

a deepest part of the recessed portion, and is not less than 10 nm.

According to a sixth aspect of the present invention, the isolation insulating film has another recessed portion shallower than the recessed portion located around the first active region, in an edge portion on the side of the second active region, the shallower recessed portion is located around the second active region.

A seventh aspect of the present invention is directed to a semiconductor device comprising: a semiconductor substrate; an isolation insulating film selectively located in a surface of the semiconductor substrate; and a first transistor located on a first active region defined by the isolation insulating film, the first transistor having a first gate insulating film of a first thickness which is selectively located on the first active region, the isolation insulating film having a first recessed portion in an edge portion on the side of the first active region, the first recessed portion being located around the first active region, a depth of the first recessed portion being defined as a vertical height between a main surface of the first active region and a deepest part of the first recessed portion and being not less than 10 nm.

According to an eighth aspect of the present invention, the semiconductor device further comprises: a second transistor located on a second active region which is defined by the isolation insulating film as being different from the first active region in the surface of the semiconductor substrate, the second transistor having a second gate insulating film of a second thickness which is selectively located on the second active region, the first thickness being greater than the second thickness, the isolation insulating film having a second recessed portion in an edge portion on the side of the second active region, the second recessed portion being located around the second active region, a depth of the second recessed portion being defined as a vertical height between a main surface of the second active region and a deepest part of the second recessed portion and being

not less than 10 nm.

According to a ninth aspect of the present invention, the semiconductor device further comprises: a second transistor located on a second active region which is defined by the isolation insulating film as being different from the first active region in the surface of the semiconductor substrate, the second transistor having a second gate insulating film of a second thickness which is selectively located on the second active region, the first thickness being greater than the second thickness, the isolation insulating film having a second recessed portion in an edge portion on the side of the second active region, the second recessed portion being located around the second active region.

According to a tenth aspect of the present invention, the first transistor includes a transistor forming an input/output circuit, and the second transistor includes a transistor forming an analog circuit.

An eleventh aspect of the present invention is directed to a method of manufacturing a semiconductor device comprising the steps of: (a) selectively forming an isolation insulating film in a surface of a semiconductor substrate to define first and second active regions; (b) forming a silicon nitride film over a whole surface; (c) removing the silicon nitride film from on the first active region and from on top of an edge portion of the isolation insulating film on the side of the first active region; (d) with a remainder of the silicon nitride film as a mask, removing the edge portion of the isolation insulating film on the side of the first active region, to form a recessed portion around an edge portion of the first active region; (e) forming an insulation film on a surface of the first active region; and (f) after removal of the remainder of the silicon nitride film, increasing the insulation film in thickness to form a first gate insulating film of a first thickness and to form on a surface of the second active region, a second gate insulating film having a thickness corresponding to an increment of the thickness of the

insulation film. The step (d) includes the step of forming the recessed portion to a depth at which threshold voltage of the first transistor is substantially constant according to a characteristic of variation in threshold voltage of the first transistor with respect to variation in depth of the recessed portion.

According to a twelfth aspect of the present invention, the depth at which threshold voltage of the first transistor is substantially constant is a depth at which a range of variation in threshold value of the first transistor is 5 to 10% of a maximum range of variation according to the characteristic of variation.

A thirteenth aspect of the present invention is directed to a method of manufacturing a semiconductor device comprising the steps of: (a) selectively forming an isolation insulating film in a surface of a semiconductor substrate to define first and second active regions; (b) forming a silicon nitride film over a whole surface; (c) removing the silicon nitride film from on the first active region and from on top of an edge portion of the isolation insulating film on the side of the first active region; (d) with a remainder of the silicon nitride film as a mask, removing the edge portion of the isolation insulating film on the side of the first active region, to form a recessed portion around an edge portion of the first active region; (e) forming an insulation film on a surface of the first active region; and (f) after removal of the remainder of the silicon nitride film, increasing the insulation film in thickness to form a first gate insulating film of a first thickness and to form on a surface of the second active region, a second gate insulating film having a thickness corresponding to an increment of the thickness of the insulation film. A depth of the recessed portion is defined as a vertical height between a main surface of the first active region and a deepest part of the recessed portion. The step (d) includes the step of forming the recessed portion to a depth of not less than 10 nm.

A fourteenth aspect of the present invention is directed to a method of manufacturing a semiconductor device comprising the steps of: (a) selectively forming an isolation insulating film in a surface of a semiconductor substrate to define first and second active regions; (b) forming an insulation film on surfaces of the first and second active regions; (c) selectively forming a resist pattern to cover the insulation film on the first active region and an edge portion of the isolation insulating film on the side of the first active region; (d) with the resist pattern as a mask, removing the insulation film on the second active region, and an edge portion of the isolation insulating film on the side of the second active region, to form a recessed portion around an edge portion of the second active region; and (e) after removal of the resist pattern, increasing the insulation film in thickness to form a first gate insulating film of a first thickness and to form on a surface of the second active region, a second gate insulating film having a thickness corresponding to an increment of the thickness of the insulation film. The step (d) includes the step of forming the recessed portion to a depth at which threshold voltage of the second transistor is substantially constant according to a characteristic of variation in threshold voltage of the second transistor with respect to variation in depth of the recessed portion.

According to a fifteenth aspect of the present invention, the depth at which threshold voltage of the second transistor is substantially constant is a depth at which a range of variation in threshold voltage of the second transistor is 5 to 10% of a maximum range of variation according to the characteristic of variation.

A sixteenth aspect of the present invention is directed to a method of manufacturing a semiconductor device comprising the steps of: (a) selectively forming an isolation insulating film in a surface of a semiconductor substrate to define first and second active regions; (b) forming an insulation film on surfaces of the first and second

active regions; (c) selectively forming a resist pattern to cover the insulation film on the first active region, and an edge portion of the isolation insulating film on the side of the first active region; (d) with the resist pattern as a mask, removing the insulation film on the second active region, and an edge portion of the isolation insulating film on the side of the second active region, to form a recessed portion around an edge portion of the second active region; and (e) after removal of the resist pattern, increasing the insulation film in thickness to form a first gate insulating film of a first thickness and to form on a surface of the second active region, a second gate insulating film having a thickness corresponding to an increment of the thickness of the insulation film. A depth of the recessed portion is defined as a vertical height between a main surface of the first active region and a deepest part of the recessed portion. The step (d) includes the step of forming the recessed portion to a depth of not less than 10 nm.

In the semiconductor device of the first aspect, the isolation insulating film has a recessed portion in an edge portion on the side of either the first or second active region, the recessed portion being located around either the first or second active region. The depth of the recessed portion is set to a depth at which the threshold voltage of either the first or second transistor is substantially constant according to the characteristic of variation in the threshold voltage of either the first or second transistor with respect to variation in the depth of the recessed portion. Therefore, even if the depth of the recessed portion varies, there would be less variation in threshold voltage due to the inverse narrow-channel effect. This improves manufacturing yield of the semiconductor device.

The semiconductor device of the second aspect can more specifically determine the depth of the recessed portion.

The semiconductor device of the third aspect can more specifically determine

the depth of the recessed portion.

The semiconductor device of the fourth aspect can reduce variation in threshold voltage due to the inverse narrow-channel effect, for example, by forming the recessed portion to such a depth as to reliably reduce the variation in threshold voltage.

The semiconductor device of the fifth aspect can more specifically determine the depth of the recessed portion.

The semiconductor device of the sixth aspect can be provided with a more practical configuration.

The semiconductor device of the seventh aspect has the first recessed portion around the first active region, the depth of the first recessed portion being defined as a vertical height between the main surface of the first active region and the deepest part of the first recessed portion and being not less than 10 nm. This reliably reduces variation in threshold voltage due to the inverse narrow-channel effect occurring in the first transistor.

The semiconductor device of the eighth aspect has the second recessed portion around the second active region, the depth of the second recessed portion being not less than 10 nm. This reliably reduces variation in threshold voltage due to the inverse narrow-channel effect occurring in the first and second transistors.

The semiconductor device of the ninth aspect has the second recessed portion around the second active region. Thus, variation in threshold voltage due to the inverse narrow-channel effect can be reduced, for example, by forming the recessed portion to such a depth as to reliably reduce the variation in threshold voltage.

The semiconductor device of the tenth aspect can achieve a configuration that is suitable for forming the analog circuit and the input/output circuit on one substrate.

The method of the eleventh aspect provides two kinds of transistors with the

first and second gate insulating films of different thickness. In the process of manufacturing, a recessed portion is formed around the edge portion of the first active region to a depth at which the threshold voltage of the first transistor is substantially constant according to the characteristic of variation in the threshold voltage of the first transistor with respect to variation in the depth of the recessed portion. Therefore, even if the depth of the recessed portion varies, there would be less variation in threshold voltage due to the inverse narrow-channel effect. This improves manufacturing yield of the semiconductor device.

The method of the twelfth aspect can more specifically determine the depth of the recessed portion.

The method of the thirteenth aspect provides two kinds of transistors with the first and second gate insulating films of different thickness. In the process of manufacturing, a recessed portion is formed to a depth of not less than 10 nm around the first active region. Therefore, even if the depth of the recessed portion varies, there would be less variation in threshold voltage due to the inverse narrow-channel effect. This improves manufacturing yield of the semiconductor device.

The method of the fourteenth aspect provides two kinds of transistors with the first and second gate insulating films of different thickness. In the process of manufacturing, a recessed portion is formed around the second active region to a depth at which the threshold voltage of the second transistor is substantially constant according to the characteristic of variation in the threshold voltage of the second transistor with respect to variation in the depth of the recessed portion. Therefore, even if the depth of the recessed portion varies, there would be less variation in threshold voltage due to the inverse narrow-channel effect. This improves manufacturing yield of the semiconductor device.

The method of the fifteenth aspect can more specifically determine the depth of the recessed portion.

The method of the sixteenth aspect provides two kinds of transistors with the first and second gate insulating films of different thickness. In the process of manufacturing, a recessed portion is formed to a depth of not less than 10 nm around the second active region. Therefore, even if the depth of the recessed portion varies, there would be less variation in threshold voltage due to the inverse narrow-channel effect. This improves manufacturing yield of the semiconductor device.

An object of the present invention is to provide a semiconductor device and a manufacturing method therefor that reduce the occurrence of variation in the threshold voltage of a MOS transistor formed by the dual oxide process, thereby to improve manufacturing yield.

These and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1 and 2 are cross-sectional views for explaining a configuration of a semiconductor device according to a first preferred embodiment of the present invention;

Figs. 3 to 11 are cross-sectional views for explaining a manufacturing process for the semiconductor device according to the first preferred embodiment of the present invention;

Fig. 12 shows part of the configuration of the semiconductor device according to the first preferred embodiment of the present invention;

Fig. 13 shows the dependency of threshold voltage on variation in the depth of

a recessed portion around an active region;

Figs. 14 and 15 are cross-sectional views for explaining a configuration of a semiconductor device according to a second preferred embodiment of the present invention;

Figs. 16 to 20 are cross-sectional views for explaining a manufacturing process for the semiconductor device according to the second preferred embodiment of the present invention;

Figs. 21 and 22 are cross-sectional views for explaining a configuration of a semiconductor device according to a third preferred embodiment of the present invention;

Figs. 23 to 27 are cross-sectional views for explaining a manufacturing process for the semiconductor device according to the third preferred embodiment of the present invention;

Figs. 28 and 29 are cross-sectional views for explaining a configuration of a conventional semiconductor device;

Figs. 30 to 34 are cross-sectional views for explaining a manufacturing process for the conventional semiconductor device; and

Fig. 35 shows part of the configuration of the conventional semiconductor device.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

<A. First Preferred Embodiment>

<A-1. Device Configuration>

Referring to Figs. 1 and 2, two kinds of MOS transistors 100 and 200 formed by a dual oxide process according to the present invention will be described.

Fig. 1 shows cross-sectional shapes of the MOS transistors 100 and 200

longitudinally of their gates, and Fig. 2 shows the cross-sectional shapes thereof transversely of the gates.

As shown in Figs. 1 and 2, the MOS transistor 100 is formed with a relatively thick gate oxide film in a thick-film portion AR, and the MOS transistor 200 is formed with a relatively thin gate oxide film in a thin-film portion BR.

The MOS transistors 100 and 200 are located in active regions 3A and 3B, respectively, which are defined by an isolation insulating film 2 formed in the surface of a semiconductor substrate 1. The isolation insulating film 2 is a kind of element isolation insulating films called STI (Shallow Trench Isolation).

In the surfaces of the active regions 3A and 3B, well regions 4A and 4B are located, respectively, and channel implant regions 5A and 5B are located in the surfaces of the well regions 4A and 4B, respectively.

On the main surface of the semiconductor substrate 1, gate oxide films GX1 and GX2 of different thickness are located in the active regions 3A and 3B, respectively, and gate electrodes GT1 and GT2 are located on top of the gate oxide films GX1 and GX2, respectively.

Further, an interlayer insulation film 6 is located to cover the gate electrodes GT1 and GT2, on top of which planarized interlayer insulation films 7 and 8 are located.

Corresponding to the MOS transistors 100 and 200, contact portions 9A and 9B are provided, respectively, passing through the interlayer insulation films 6 to 8. As shown in Fig. 2, the contact portions 9A and 9B are electrically connected to source/drain regions SDA and SDB of the MOS transistors 100 and 200, respectively. Further as shown, sidewall oxide films GW1 and GW2 are located on the side faces of the gate electrodes GT1 and GT2, respectively.

The gate electrodes GT1 and GT2 are also connected to the contact portions,

which is however not shown in Fig. 2 for convenience's sake.

As shown in Figs. 1 and 2, the isolation insulating film 2 which defines the active region 3A in the thick-film portion AR has an excessively removed edge portion on the side of the MOS transistor 100 and thereby a recessed portion DP is formed in the edge portion of the active region 3A. On the other hand, an edge portion of the isolation insulating film 2 on the side of the MOS transistor 200 in the thin-film portion BR is not removed very much, and even if it is removed, the amount of removal is very little and a resultant recess is much shallower than the recessed portion DP in the thick-film portion AR.

<A-2. Manufacturing Method>

Next, a method of manufacturing the MOS transistors 100 and 200 will be described step by step with reference to Figs. 3 to 11.

In a step of Fig. 3, the isolation insulating film 2 is selectively formed in the surface of the semiconductor substrate 1 to define the active regions 3A and 3B.

In a step of Fig. 4, after an oxide film OX11 is formed by thermal oxidation on the active regions 3A and 3B, the well regions 4A, 4B and the channel implant regions 5A, 5B are formed by impurity ion implantation, more specifically well formation and channel doping, in the active regions 3A and 3B.

In the well formation, for formation of a p-well region, boron ions as impurities are implanted in both the active regions 3A and 3B with an energy of 200 to 500 keV at a dose of 5×10^{12} to $1\times10^{14}/cm^2$.

Then, boron ions are further implanted with an energy of 80 to 160 keV at a dose of 3×10^{12} to $2\times10^{15}/cm^2$ to form a channel cut layer.

In the channel doping, boron ions are implanted in the active region 3A with an energy of 15 to 70 keV at a dose of 3×10^{12} to $5\times10^{13}/cm^2$ and implanted in the

active region 3B with an energy of 15 to 70 keV at a dose of 5×10^{12} to $1\times10^{14}/cm^2$. In Fig. 4, the channel cut layer integrated with the channel implant regions is shown as the channel implant regions 5A and 5B. The same can be said of the other drawings.

For formation of an n-well region, on the other hand, phosphorus ions as impurities are implanted in both the active regions 3A and 3B with an energy of 300 to 1,000 keV at a dose of 5×10^{12} to $1\times10^{14}/cm^2$.

Then, phosphorus ions are further implanted with an energy of 160 to 400 keV at a dose of 3×10^{12} to $2\times10^{13}/cm^2$ to form a channel cut layer.

In the channel doping, arsenic ions are implanted in the active region 3A with an energy of 15 to 70 keV at a dose of 3×10^{12} to $5\times10^{13}/cm^2$ and implanted in the active region 3B with an energy of 50 to 200 keV at a dose of 5×10^{12} to $1\times10^{14}/cm^2$.

In a step of Fig. 5, a silicon nitride film SN1 is formed to a thickness of 5 to 30 nm (50-300 Å) over the whole surface.

In a step of Fig. 6, the silicon nitride film SN1 is selectively removed by wet etching so that only the silicon nitride film SN1 in the thick-film portion AR is removed.

In a step of Fig. 7, by wet etching of the silicon oxide film with the silicon nitride film SN1 as a mask, the oxide film OX11 in the thick-film portion AR is removed and also the edge portion of the isolation insulating film 2 is removed. Thereby a deep recessed portion DP is formed around the active region 3A.

In a step of Fig. 8, with the silicon nitride film SN1 left in the thin-film portion BR, an oxide film OX13 of a third thickness is formed only on the surface of the active region 3A. Here, the "third thickness" is defined as a resultant thickness of subtraction of a second thickness from a first thickness, where the first thickness (4-12 nm) and the second thickness (1-4 nm) are respectively the thicknesses of the gate oxide films GX1 and GX2 to be formed later.

In a step of Fig. 9, the silicon nitride film SN1 in the thin-film portion BR is removed by etching. This etching is conditioned not to remove the silicon oxide film; therefore, the silicon oxide film is hardly removed from the thick-film portion AR and the thin-film portion BR.

Although the isolation insulating film 2 and the oxide film OX13 in the thick-film portion AR are slightly removed by the removal of the oxide film OX11 from the active region 3B, the thickness of the oxide film OX11 is so small that there is little influence. Alternatively, the influence of the removal of the oxide film OX11 can be cancelled by increasing the thickness of the oxide film OX13 by the thickness of the oxide film OX11.

In a step of Fig. 10, the oxide film OX13 is increased in thickness by thermal oxidation or chemical vapor deposition (CVD) to form the gate oxide film GX1 of the first thickness on the active region 3A. At this time, the gate oxide film GX2 of the second thickness is formed on the active region 3B.

In a step of Fig. 11, a conducting layer CL to be the gate electrodes GT1 and GT2 is formed to cover the gate oxide films GX1 and GX2.

The conducting layer CL is then patterned to form the gate electrodes GT1 and GT2. With the gate electrodes GT1 and GT2 as masks, ion implantation is carried out to form the source/drain regions SDA and SDB in the active regions 3A and 3B, respectively.

Here the source/drain implants are performed under the conditions that for formation of a p-well region, arsenic ions are implanted with an energy of 3 to 100 keV at a dose of 1×10^{15} to $6\times10^{15}/cm^2$, while for formation of an n-well region, boron ions are implanted with an energy of 1 to 20 keV at a dose of 1×10^{15} to $6\times10^{15}/cm^2$.

After the interlayer insulation films 6 to 8 are laminated one above the other

over the whole surface, the contact portions 9A and 9B are formed, reaching the source/drain regions SDA and SDB respectively through the interlayer insulation films 6 to 8. This provides the MOS transistors 100 and 200 shown in Figs. 1 and 2.

<A-3. Effects>

Fig. 12 shows the details of a region Y in Fig. 8. As shown in Fig. 12, a depth L of the recessed portion DP around the active region 3A at this stage should preferably be about 10 nm (100 Å) at the minimum, the depth being defined as a depth between the main surface of the active region 3A and the deepest part of the recessed portion DP. For that, it is desirable that the depth L of the recessed portion DP formed in the step of Fig. 8 be determined in consideration of lowering of the main surface level of the active region 3A by the formation of the oxide film OX13.

Now, why the depth L of the recessed portion DP around the active region 3A should be at least about 10 nm will be described hereinbelow.

Fig. 13 shows the relationship between the threshold voltage (Vth) of a MOS transistor and the depth of a recess in the edge portion of STI (isolation insulating film 2), i.e., the depth of a recess around the active region.

In Fig. 13, the horizontal axis indicates the depth (nm) of a recess around the active region, and the vertical axis indicates the threshold voltage (V) of a MOS transistor. The depth of a recess being 0 corresponds to a case where the edge portion of STI is not excessively removed, i.e., it corresponds to a design value.

As shown in Fig. 13, when the depth of a recess around the active region is relatively shallow, e.g., shallower than 10 nm, there occur considerable variations in threshold voltage due to an inverse narrow-channel effect responsive to variations in the depth of the recess. More specifically, a range of variation in threshold voltage responsive to the 10-nm range of variation in the depth of a recess is close to 0.2 to 0.3 V

which is the maximum range of variation.

The maximum range of variation corresponds to a difference between the threshold voltage at a depth (i.e., point P in Fig. 13) that causes little variation (substantially constant) in threshold voltage as the depth of a recess increases, and the threshold voltage when the depth of the recess is 0 (i.e., point Q in Fig. 13).

Conventionally it has been known that the threshold voltage depends upon the depth of a recess around the active region, but there is little understanding of the exact characteristics thereof. Conventional MOS transistors therefore have been formed with a relatively shallow recess (about 4-7 nm) as indicated by an area D1 of Fig. 13.

The inventors of the present invention, on the other hand, have made a wide range of variations in the depth of a recess, thereby to obtain data about the dependency of threshold value as graphically shown in Fig. 13.

The inventors have then reached a conclusion that as shown in Fig. 13, if a recess around the active region has a relatively great depth of 10 nm or more, there would occur little variation in threshold voltage even if the depth of the recess somewhat varies as indicated by an area D2.

When the depth of a recess around the active region is 10 nm or more, a range of variation in threshold value is 0.03 to 0.04 V which is about 5 to 10 % of the maximum range of variation.

By forming the recessed portion DP around the active region 3A to a depth of at least about 10 nm, the occurrence of variation in threshold value due to the inverse narrow-channel effect can be reduced even if the depth of the recessed portion DP varies. This improves manufacturing yield of the semiconductor device.

In consideration of variations in manufacture, the recessed portion DP in each semiconductor device should be of a depth of 10 nm or more, even in the semiconductor

device with the shallowest recessed portion DP.

Although some variation in threshold voltage occurs in the MOS transistor 100, the thick gate oxide film GX1 (4-12 nm), high driving voltage of 1.8 to 5 V, and high threshold voltage of 0.4 to 1.5 V of the MOS transistor 100 makes the allowable range of variation in threshold voltage wider than that for the MOS transistor 200 formed in the thin-film portion BR; therefore, there is little influence on manufacturing yield.

In order to form the recessed portion DP to a depth of about 10 nm around the active region 3A, the time for wet etching in the step of Fig. 7 should be lengthened than before.

For example, if a conventional etching process produces a recessed portion of about 5 nm in depth, the recessed portion DP of about 10 nm in depth can be formed by doubling the conventional etch time.

The MOS transistor 100 is suitable for circuit portions which require a relatively high threshold voltage (5-10 V), such as an input/output circuit (including individual input and output circuits).

In the MOS transistor 200 in the thin-film portion BR shown in Fig. 1, there is no recess around the active region 3B. Therefore, no reduction in the threshold voltage of the MOS transistor 200 occurs due to the inverse narrow-channel effect.

From this, the MOS transistor 200 is suitable as MOS transistors such as a logic circuit or the like which require a high-speed operation (gate oxide film thickness: 1-4 nm; driving voltage: 0.8-1.8 V; threshold voltage: 0.15-0.6 V).

The driving voltage for an input/output circuit is normally 2.5 V or 3.3 V, which is converted into a voltage of 0.8 to 1.8 V by an internal circuit to be used as a driving voltage for a logic circuit or the like.

While the thick-film portion AR, as above described, is suitable for forming a

semiconductor element constituting an input/output circuit, the thin-film portion BR is also suitable for forming a semiconductor element constituting an analog circuit.

More specifically, the analog circuit requires high transconductance to ensure gain. When the analog circuit and the input/output circuit are formed on one substrate, use of the MOS transistor 200 in the thin-film portion BR which has a low threshold voltage in the analog circuit increases transconductance, thereby achieving high gain. Further, variations in the threshold voltage can be reduced by controlling the formation of a recess around the active region 3B in the thin-film portion BR, which ensures steady transistor performance.

<B. Second Preferred Embodiment>

<B-1. Device Configuration>

Referring now to Figs. 14 and 15, two kinds of MOS transistors 300 and 400 formed by the dual oxide process according to the present invention will be described.

Fig. 14 shows cross-sectional shapes of the MOS transistors 300 and 400 longitudinally of their gates, and Fig. 15 shows cross-sectional shapes thereof transversely of their gates.

Referring to Figs. 14 and 15, the MOS transistor 300 is formed with a relatively thick gate oxide film in the thick-film portion AR, and the MOS transistor 400 is formed with a relatively thin gate oxide film in the thin-film portion BR.

As shown in Figs. 14 and 15, the isolation insulating film 2 which defines the active region 3B in the thin-film portion BR has an excessively removed edge portion on the side of the MOS transistor 400 and thereby a recessed portion DP is formed in the edge portion of the active region 3B. On the other hand, the edge portion of the isolation insulating film 2 on the side of the MOS transistor 300 in the thick-film portion AR is not excessively removed.

The other parts of identical configuration to those of the MOS transistors 100 and 200 described with reference to Figs. 1 and 2 are denoted by the same reference numerals or characters and the description thereof will be omitted.

<B-2. Manufacturing Method>

Next, a method of manufacturing the MOS transistors 300 and 400 will be described step by step with reference to Figs. 16 to 20.

In a step of Fig. 16, the isolation insulating film 2 is selectively formed in the surface of the semiconductor substrate 1 to define the active regions 3A and 3B. After formation of a thermal oxide film (not shown), the well regions 4A, 4B and the channel implant regions 5A, 5B are formed by impurity ion implantation, more specifically well formation and channel doping, in the active regions 3A and 3B.

The well formation and the ion implantation for forming a channel cut layer are performed under the same conditions as described in the first preferred embodiment. The same can be said of the channel doping.

In a step of Fig. 17, the main surfaces of the active regions 3A and 3B are thermally oxidized to form the oxide film OX13 of a third thickness. Here the "third thickness" is defined as a resultant thickness from subtraction of a second thickness from a first thickness, where the first and second thicknesses are respectively the thicknesses of the gate oxide films GX1 and GX2 to be formed later.

In a step of Fig. 18, a resist pattern RM11 is formed by a photolithographic technique to cover the thick-film portion AR.

Then, the oxide film OX13 in the thin-film portion BR is removed by wet etching which is performed for a longer period of time than the conventional predetermined period of time, whereby a deep recessed portion DP is formed around the active region 3A. For example, if a conventional etching process produces a recessed

portion of about 5 nm in depth, the recessed portion DP of about 10 nm in depth can be formed by doubling the conventional etch time.

After removal of the resist pattern RM11, in a step of Fig. 19, the oxide film OX13 is increased in thickness by thermal oxidation or CVD to form the gate oxide film GX1 of the first thickness on top of the active region 3A. At this time, the gate oxide film GX2 of the second thickness is formed on top of the active region 3B.

In a step of Fig. 20, the conducting layer CL to be the gate electrodes GT1 and GT2 is formed to cover the gate oxide films GX1 and GX2.

The conducting layer CL is then patterned to form the gate electrodes GT1 and GT2. With the gate electrodes GT1 and GT2 as masks, ion implantation is carried out to form the source/drain regions SDA and SDB in the active regions 3A and 3B, respectively.

Here the source/drain implants are performed under the same conditions as described in the first preferred embodiment.

After the interlayer insulation films 6 to 8 are laminated one above the other over the whole surface, the contact portions 9A and 9B are formed, reaching the source/drain regions SDA and SDB respectively through the interlayer insulation films 6 to 8. This provides the MOS transistors 300 and 400 shown in Figs. 14 and 15.

<B-3. Effects>

The depth of the recessed portion DP around the active region 3B at the stage of Fig. 19 should preferably be about 10 nm (100 Å) at the minimum, the depth being defined as a depth between the main surface of the active region 3B and the deepest part of the recessed portion DP. For that, it is desirable that the depth of the recessed portion DP formed in the step of Fig. 18 be determined in consideration of lowering of the main surface level of the active region 3B by the formation of the oxide film OX13.

In order to form the recessed portion DP to a depth of about 10 nm around the active region 3B, the time for wet etching in the step of Fig. 17 should be lengthened than before.

For example, if a conventional etching process produces a recessed portion of about 5 nm in depth, the recessed portion DP of about 10 nm can be formed by doubling the conventional etch time.

By forming the recessed portion DP to a depth of at least about 10 nm around the active region 3B, the occurrence of variation in threshold voltage due to the inverse narrow-channel effect can be reduced even if the depth of the recessed portion DP varies. This improves manufacturing yield of the semiconductor device, the reason of which is the same as described in the first preferred embodiment.

In the MOS transistor 300 in the thick-film portion AR shown in Fig. 14, there is little recess around the edge of the active region 3A and very little, if any at all. Therefore, no reduction in the threshold voltage of the MOS transistor 300 occurs due to the inverse narrow-channel effect.

From this, the MOS transistor 300 is for example suitable for a memory cell in an eRAM (embedded RAM), which brings about the effect of controlling problems such as deterioration of sub-leakage current and refresh capability.

While the thick-film portion AR, as has been described in the first preferred embodiment, is suitable for forming a semiconductor element constituting an input/output circuit, the thin-film portion BR is also suitable for forming a semiconductor element constituting an analog circuit.

More specifically, the analog circuit requires high transconductance to ensure gain. When the analog circuit and the input/output circuit are formed on one substrate, use of the MOS transistor 400 in the thin-film portion BR which has a low threshold

voltage in the analog circuit increases transconductance, thereby achieving high gain. Further, variations in the threshold voltage can be reduced by forming the recessed portion DP of at least about 10 nm around the active region 3B in the thin-film portion BR, which ensures steady transistor performance.

<C. Third Preferred Embodiment>

<C-1. Device Configuration>

Referring now to Figs. 21 and 22, two kinds of MOS transistors 500 and 600 formed by the dual oxide process according to the present invention will be described.

Fig. 21 shows cross-sectional shapes of the MOS transistors 500 and 600 longitudinally of their gates, and Fig. 22 shows cross-sectional shapes thereof transversely of their gates.

Referring to Figs. 21 and 22, the MOS transistor 500 is formed with a relatively thick gate oxide film in the thick-film portion AR, and the MOS transistor 600 is formed with a relatively thin gate oxide film in the thin-film portion BR.

As shown in Figs. 21 and 22, the isolation insulating film 2 which defines the active regions 3A and 3B in the thick-film portion AR and the thin-film portion BR has excessively removed edge portions on the sides of the MOS transistors 500 and 600. Thus, recessed portions (first and second recessed portions) DP are formed in the edge portions of the active regions 3A and 3B.

The other parts that are identical in configuration to those of the MOS transistors 100 and 200 described with reference to Figs. 1 and 2 are denoted by the same reference numerals or characters and the description thereof will be omitted.

<C-2. Manufacturing Method>

Next, a method of manufacturing the MOS transistors 500 and 600 will be described step by step with reference to Figs. 23 to 27.

First, after the oxide film OX11 is formed by thermal oxidation on the active regions 3A and 3B through the processes described with reference to Figs. 3 and 4, the well regions 4A, 4B and the channel implant regions 5A, 5B are formed by impurity ion implantation, more specifically, by well formation and channel doping, in the active regions 3A and 5B.

In a step of Fig. 23, by wet etching of the silicon oxide film, the oxide film OX11 is removed and also the edge portion of the isolation insulating film 2 is removed. Thereby deep recessed portions DP are formed around the active regions 3A and 3B.

In a step of Fig. 24, the silicon nitride film SN1 is formed to a thickness of 5 to 30 nm (50-300 Å) over the whole surface.

In a step of Fig. 25, the silicon nitride film SN1 is selectively removed by wet etching so that only the silicon nitride film SN1 in the thick-film portion AR is removed and, with the silicon nitride film SN1 left in the thin-film portion BR, the oxide film OX13 of a third thickness is formed only on the surface of the active region 3A. Here, the "third thickness" is defined as a resultant thickness of subtraction of a second thickness from a first thickness, where the first thickness and the second thickness are respectively the thicknesses of the gate oxide films GX1 and GX2 to be formed later.

In a step of Fig. 26, the silicon nitride film SN1 remaining in the thin-film portion BR is removed by etching. This etching is performed on the condition that the silicon oxide film is not removed, so that little silicon oxide film is removed from the thick-film portion AR and the thin-film portion BR. Then, the oxide film OX13 is increased in thickness by thermal oxidation or CVD thereby to form the gate oxide film GX1 of the first thickness on top of the active region 3A. At this time, the gate oxide film GX2 of the second thickness is formed on top of the active region 3B.

In a step of Fig. 27, the conducting layer CL to be the gate electrodes GT1 and

GT2 is formed to cover the gate oxide films GX1 and GX2.

The conducting layer CL is then patterned to form the gate electrodes GT1 and GT2. With the gate electrodes GT1 and GT2 as masks, ion implantation is carried out to form the source/drain regions SDA and SDB in the active regions 3A and 3B, respectively.

Here the source/drain implants are performed under the same conditions as described in the first preferred embodiment.

After the interlayer insulation films 6 to 8 are laminated one above the other over the whole surface, the contact portions 9A and 9B are formed which reach the source/drain regions SDA and SDB respectively through the interlayer insulation films 6 to 8. This provides the MOS transistors 500 and 600 shown in Figs. 21 and 22.

<C-3. Effects>

The depth of the recessed portions DP around the active regions 3A and 3B at the stage of Fig. 26 should preferably be about 10 nm (100 Å) at the minimum, the depth being defined as a depth between the main surfaces of the active regions 3A and 3B and the deepest part of the recessed portions DP. For that, it is desirable that the depth of the recessed portions DP formed in the step of Fig. 23 be determined in consideration of lowering of the main surface level of the active regions 3A and 3B by the formation of the oxide film OX13 and the gate oxide film GX2.

In order to form the recessed portions DP to a depth of about 10 nm around the active regions 3A and 3B, the time for wet etching in the step of Fig. 23 should be lengthened than before.

For example, if the conventional etching process produces recessed portions of about 5 nm in depth, the recessed portions DP of about 10 nm can be formed by doubling the conventional etch time.

By forming the recessed portions DP to a depth of at least about 10 nm around the active regions 3A and 3B, the occurrence of variation in threshold voltage due to the inverse narrow-channel effect can be reduced even if the depth of the recessed portion DP varies. This improves manufacturing yield of the semiconductor device, the reason of which is the same as described in the first preferred embodiment.

While the thick-film portion AR, as has been described in the first preferred embodiment, is suitable for forming a semiconductor element constituting an input/output circuit, the thin-film portion BR is also suitable for forming a semiconductor element constituting an analog circuit.

More specifically, the analog circuit requires high transconductance to ensure gain. When the analog circuit and the input/output circuit are formed on one substrate, use of the MOS transistor 600 in the thin-film portion BR which has a low threshold voltage in the analog circuit increases transconductance, thereby achieving high gain. Further, variations in the threshold voltage can be reduced by forming the recessed portion DP of at least about 10 nm around the active region 3B in the thin-film portion BR, which ensures steady transistor performance.

While the invention has been shown and described in detail, the foregoing description is in all aspects illustrative and not restrictive. It is therefore understood that numerous modifications and variations can be devised without departing from the scope of the invention.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate;

an isolation insulating film selectively located in a surface of said semiconductor substrate; and

first and second transistors located respectively on first and second active regions which are defined by said isolation insulating film,

said first transistor having a first gate insulating film of a first thickness which is selectively located on said first active region,

said second transistor having a second gate insulating film of a second thickness which is selectively located on said second active region,

said first thickness being greater than said second thickness,

said isolation insulating film having a recessed portion in an edge portion on the side of either said first or second active region,

said recessed portion being located around either said first or second active region,

a depth of said recessed portion being defined as a depth at which threshold voltage of either said first or second transistor is substantially constant according to a characteristic of variation in threshold voltage of either said first or second transistor with respect to variation in depth of said recessed portion.

2. The semiconductor device according to claim 1, wherein

a depth at which threshold voltage of either said first or second transistor is substantially constant is a depth at which a range of variation in threshold voltage of either said first or second transistor is 5 to 10% of a maximum range of variation

according to said characteristic of variation.

3. The semiconductor device according to claim 1, wherein

a depth of said recessed portion is defined as a vertical height between a main surface of said first active region and a deepest part of said recessed portion, and is not less than 10 nm.

4. A semiconductor device comprising:

a semiconductor substrate;

an isolation insulating film selectively located in a surface of said semiconductor substrate; and

first and second transistors located respectively on first and second active regions which are defined by said isolation insulating film,

said first transistor having a first gate insulating film of a first thickness which is selectively located on said first active region,

said second transistor having a second gate insulating film of a second thickness which is selectively located on said second active region,

said first thickness being greater than said second thickness,

said isolation insulating film having a recessed portion in an edge portion on the side of said first active region,

said recessed portion being located around said first active region.

5. The semiconductor device according to claim 4, wherein

a depth of said recessed portion is defined as a vertical height between a main surface of said first active region and a deepest part of said recessed portion, and is not

less than 10 nm.

6. The semiconductor device according to claim 5, wherein

said isolation insulating film has another recessed portion shallower than said recessed portion located around said first active region, in an edge portion on the side of said second active region,

said shallower recessed portion is located around said second active region.

7. A semiconductor device comprising:

a semiconductor substrate;

an isolation insulating film selectively located in a surface of said semiconductor substrate; and

a first transistor located on a first active region defined by said isolation insulating film,

said first transistor having a first gate insulating film of a first thickness which is selectively located on said first active region,

said isolation insulating film having a first recessed portion in an edge portion on the side of said first active region, said first recessed portion being located around said first active region,

a depth of said first recessed portion being defined as a vertical height between a main surface of said first active region and a deepest part of said first recessed portion and being not less than 10 nm.

8. The semiconductor device according to claim 7, further comprising:

a second transistor located on a second active region which is defined by said

isolation insulating film as being different from said first active region in the surface of said semiconductor substrate,

said second transistor having a second gate insulating film of a second thickness which is selectively located on said second active region,

said first thickness being greater than said second thickness,

said isolation insulating film having a second recessed portion in an edge portion on the side of said second active region, said second recessed portion being located around said second active region,

a depth of said second recessed portion being defined as a vertical height between a main surface of said second active region and a deepest part of said second recessed portion and being not less than 10 nm.

9. The semiconductor device according to claim 7, further comprising:

a second transistor located on a second active region which is defined by said isolation insulating film as being different from said first active region in the surface of said semiconductor substrate,

said second transistor having a second gate insulating film of a second thickness which is selectively located on said second active region,

said first thickness being greater than said second thickness,

said isolation insulating film having a second recessed portion in an edge portion on the side of said second active region, said second recessed portion being located around said second active region.

10. The semiconductor device according to claim 1, wherein

said first transistor includes a transistor forming an input/output circuit, and

said second transistor includes a transistor forming an analog circuit.

11. The semiconductor device according to claim 7, wherein
said first transistor includes a transistor forming an input/output circuit, and
said second transistor includes a transistor forming an analog circuit.

12. The semiconductor device according to claim 6, wherein
said first transistor includes a transistor forming an input/output circuit, and
said second transistor includes a transistor forming an analog circuit.

13. The semiconductor device according to claim 9, wherein
said first transistor includes a transistor forming an input/output circuit, and
said second transistor includes a transistor forming an analog circuit.

ABSTRACT OF THE DISCLOSURE

A semiconductor device and a manufacturing method therefor reduce the occurrence of variation in threshold voltage of a MOS transistor formed by a dual oxide process, thereby to improve manufacturing yield. On the main surface of a semiconductor substrate (1), gate oxide films (GX1, GX2) of different thickness are located in active regions (3A, 3B), respectively, and gate electrodes (GT1, GT2) are located on top of the gate oxide films (GX1, GX2), respectively. An isolation insulating film (2) which defines the active region (3A) in a thick-film portion (AR) has an excessively removed edge portion on the side of a MOS transistor (100) and thereby a recessed portion (DP) is formed in the edge portion of the active region (3A). On the other hand, an edge portion of the isolation insulating film (2) in a thin-film portion (BR) on the side of a MOS transistor (200) is not excessively removed.

APPENDIX B

Related Pending Application
Related Case Serial No: 09/340,504
Related Case Filing Date:

Our Ref.: MD-691 (513823)

TITLE OF THE INVENTION

A SEMICONDUCTOR DEVICE AND A METHOD OF MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention relates to a semiconductor device and a method of manufacturing the device, in particular, a structure of isolation in a semiconductor device.

DISCUSSION OF BACKGROUND

In accordance with development of integrated circuit design and process technologies, it becomes possible to manufacture an integrated circuit (IC) in which a memory element of high density and an operational circuit of high density are equipped in a single chip, whereby microminiaturization and high efficiency of a device is increasingly proceeded. Particularly, a highly integrated logic circuit (hereinbelow, referred to as logic circuit) represented by a microprocessing unit (MPU) and a dynamic random access memory (DRAM) are formed in a single chip to thereby form a logic consolidating dynamic random access memory. In producing such a logic consolidating DRAM, it is necessary to fabricate a plurality of MOS elements, respectively having different purposes, in the single chip. Therefore, the production is controlled to obtain desired

transistor characteristics in correspondence with these purposes by changing the film thickness of a gate oxide film.

In such a semiconductor device, isolation for insulating elements is preferably attained by trench isolation, which can extremely reduce an occupying area and a parasitic capacitance in comparison with the other isolation for insulating. Such trench isolation is effective for high integration and high speed. The trench isolation is formed by embedding a silicon oxide film in a groove by a chemical vapor deposition (CVD) method and etching its surface to leave the silicon oxide film only in the groove after forming the groove on a surface of a semiconductor substrate to be an isolation area, wherein the CVD method is suitable for microminiaturization in comparison with a case that a separation film is formed by thermal oxidation because it can restrict a decrement of active region caused by bird's beaks and control the shape of the trench isolation.

Figure 20 is a cross-sectional view for showing elements of the conventional semiconductor device, in which a DRAM memory cell and a logic circuit are formed on a single semiconductor substrate. In Figure 20, numerical reference 101 designates a semiconductor substrate; numerical reference 102 designates a groove, numerical references 103 and 104 designate silicon oxide

films; numerical references 1051 and 1052 designate gate oxide films; numerical reference 106 designates a polysilicon layer; numerical references 1061 and 1062 designate inter-layer insulating films; numerical reference 107 designates a metallic silicide layer; numerical reference 108 designates a side wall; numerical reference 109 designates a gate electrode; numerical references 1010 through 1013 designate source/drain areas; numerical reference 1018 designates a storage node; numerical reference 1019 designates a capacitor insulating film; numerical reference 1020 designates a cell plate; and numerical reference 1022 designates a capacitor composed of the storage node 1018, the capacitor insulating film 1019, and the cell plate 1020. Trench isolation is composed of the groove 102, and the silicon oxide film 103 and 104, by which active regions are separated. The gate electrode 109 is composed of the polysilicon layer 106, the metallic silicide layer 107, and so on.

The source/drain layer 1011 and the gate electrode 109 are horizontally overlap each other and interposed by a gate oxide film 1051. When a degree of microminiaturization is enhanced, the proportion of the width of overlapping to a memory cell becomes large. Therefore, for example in a case of nMOS, a high electric field was generated on a surface of the source/drain area 1011 and a leakage current caused by band to band

tunneling (BTBT) was sometimes generated between the capacitor 1022 and the semiconductor substrate 101 in reference X of Figure 20 when a voltage higher than that to the gate electrode 109 was applied to the source/drain area 1011. Non-flow of the leakage current is the most important characteristic in DRAM memory cells. Because when the leakage current is generated, refresh characteristics are deteriorated to cause problems in aspects of power consumption and reliability, it is necessary to reduce a mutual influence between the gate electrode 109 and the source/drain area 1011 by making the thickness of gate oxide film 1051 about 7 through 10 nm when the gate length L_1 of the DRAM memory cell is about 0.2 μm.

A high-speed transistor having a great driving capability is required in portions other than the memory cell such as a logic element and a peripheral circuit of DRAM, wherein it is the most important characteristic that an on-current sufficiently flows. Thus, gate oxide films 1052 of transistors in a logic circuit were formed to be thinner than gate oxide films 1051 of transistors in a DRAM memory cell by 3 nm in a case that the gate length L_2 was about 0.2 μm to suppress a leakage current in a memory cell and to enhance a driving capability in portions other than the memory cell.

However, the conventional device had problems that when gate oxide films having different film thicknesses

were formed on a single semiconductor substrate, silicon oxide films embedded in insides of grooves formed on the semiconductor substrate to serve as trench isolation was dropped into the grooves along the side walls of the grooves at positions adjacent to active regions in a portion other than the memory cell.

Figure 21 is a cross-sectional view for showing an element of the conventional semiconductor device which enlarges reference Y in Figure 20. As shown, although the silicon oxide film 104 embedded in an inside of the groove 2 is properly formed in the memory cell, the silicon oxide film 104 is dropped along an interface between the active region and the groove 102 in the logic circuit.

Figures 22 through 27 are cross-sectional views for illustrating steps of manufacturing the conventional semiconductor device, wherein numerical reference 1031 designates a silicon oxide film and numerical reference 1021 designates a silicon nitride film. At first, the silicon oxide film 1031 and the silicon nitride film 1021 are formed on a surface of a semiconductor substrate 101; the silicon nitride film 1021 is patterned to have openings for grooves 102 using a photoresist mask (not shown); and the grooves 102 are formed using the patterned silicon nitride film 1021 as a mask. Figure 22 is a cross-sectional view of the semiconductor device after this step.

In Figure 23, numerical references 103 and 104 are silicon oxide films. After forming the silicon oxide film 103 in the grooves 102 by thermal oxidation, the silicon oxide film 104 is embedded in the grooves 102 by a CVD method. Figure 23 is a cross-sectional view of the semiconductor device after this step. Finally, a surface of the silicon oxide film 104 is planarized by a chemical mechanical polishing (CMP), the silicon nitride film 1021 and the silicon oxide film 1031 are removed, whereby trench isolation is completed. Figure 24 is a cross-sectional view after this step.

In Figure 25, numerical reference 1053 designates a gate oxide film, and numerical reference 1042 designates a resist pattern. After forming the gate oxide film 1053 having a thickness of about 3 through 6 nm on a whole surface by thermal oxidation, the resist pattern 1042 for covering an active region of a DRAM memory cell is formed; and a part of the gate oxide film 1053 on a surface of an active region of the logic circuit is removed using the resist pattern 1042 as a mask. Figure 25 is a cross-sectional view of the semiconductor device after this step. As illustrated, because the part of the gate oxide film 1053 in the logic circuit is removed and the other part of the gate oxide film 1053 in the memory cell is left, the silicon oxide film 104 is shaped to drop into the grooves along an interface between the gate oxide film 1053 and the grooves 102 in the logic circuit.

After removing the resist pattern 1042, a gate oxide film 1052 having a thickness of about 4 through 7 nm is formed again on a whole surface by thermal oxidation; and gate electrodes 109 are formed. Figure 26 is a cross-sectional view for illustrating element of the semiconductor device after this step.

Thereafter, a side wall 108, source/drain areas 1010 and 1011, source/drain areas 1012 and 1013, an inter-layer insulating film 1061, a contact hole 1016, a wire 1017, an inter-layer insulating film 1062, a contact hole 23, a storage node 1018, a capacitor insulating film 1019, and a cell plate 1020 are formed thereon, whereby the semiconductor device shown in Figure 20 is fabricated.

Figure 27 is a cross-sectional view taken along a line Z-Z of Figure 26. A drop 190 shown in Figure 27 may be produced along all interfaces between the grooves 102 and the gate oxide film 1052 in the logic circuit, wherein when the silicon oxide film 104 was dropped, an inverse narrow channel effect occurred by concentration of electric fields in an end of the active region under the gate electrode, whereby there was a problem that a threshold voltage was decreased.

Conventional techniques are described in JP-A-3-99430, in which a method of manufacturing a semiconductor device having a CMOS structure for conducting ion channeling by injecting ions using a silicon oxide film

and a silicon nitride film as masks, and JP-A-9-74072, in which a method of manufacturing a semiconductor device having a CMOS structure for injecting to a well and injecting ions into a gate electrode using a single mask, wherein these techniques are for the semiconductor devices having uniform film thicknesses of gate oxide films.

SUMMARY OF THE INVENTION

It is an object of the present invention to solve the above mentioned problems inherent in the conventional technique and to provide a semiconductor device in which a silicon oxide film at a position along an edge of a groove is not dropped; shapes of end portions of active regions in contact with trench isolation can be made substantially the same; properties of transistors are not affected by the shapes of the active regions; and miniaturization of a chip is realized with maintaining preferable properties of elements, even though the transistors having different film thicknesses of gate oxide films are included in a DRAM memory cell, a logic circuit and so on in a single conductor substrate, and to provide a method of manufacturing such a semiconductor device.

According to the first aspect of the present invention, there is provided a semiconductor device comprising: grooves formed on a main surface of a semiconductor substrate, a silicon oxide film embedded in

insides of the grooves, a first active region disposed on a first portion of the main surface of the semiconductor substrate interposed between the grooves, first field effect transistors having a first gate oxide film formed on the main surface of the first active region, a second active region having the same shapes of end portions as those of the first active region, disposed between the grooves in a second portion of the main surface of the semiconductor substrate, second field effect transistors having a second gate oxide film of a film thickness different from that of the first gate oxide film formed on the main surface of the second active region, whereby a part of the silicon oxide film along an edge of a groove is not dropped even though the gate oxide films respectively having different film thicknesses are formed on surfaces of a plurality of active regions in a single chip; and transistor properties are not affected by shapes of the active regions because shapes of end portions of the active regions in contact with trench isolation are made substantially the same.

According to a second aspect of the present invention, there is provided a semiconductor device, wherein: the widths of the grooves interposing the first active region and the second active region are the same; and the heights from the bottom surfaces of the grooves to surfaces of the silicon oxide films are the same, whereby because it becomes possible that a margin of

depth of focus is assured in a photolithographing process when the gate electrode above this surface is patterned, a short caused by a material of the gate electrode remained at a time of etching the material deposited on the surface of the second silicon oxide film does not occur; it also does not occur that a surface of the semiconductor substrate is etched so as to protrude an etching stopper of the gate oxide film by excessive etching for completely removing the material of the gate electrode.

According to a third aspect of the present invention, there is provided a semiconductor device, further comprising: an inter-layer insulating film having openings reaching the first field effect transistors formed on surfaces of the first field effect transistors, and capacitors connected to the first field effect transistors through the openings, wherein the first gate oxide films are thicker than the second gate oxide films, whereby it becomes possible to form a DRAM having a good refresh property by suppressing leakage currents using the thick gate oxide film and a logic circuit having a high driving capability resulted from the thin gate oxide film and restricting a decrement of a threshold voltage by suppressing an advance narrow channel effect in a single chip.

According to a forth aspect of the present invention, there is provided a method of manufacturing a

semiconductor device, comprising steps of: forming grooves surrounding a first active region and a second active region respectively disposed on a main surface of a semiconductor substrate, forming a first silicon oxide film for embedding the grooves, forming a second silicon oxide film for covering the first active region and the second active region, forming a first mask, having openings on a main surface of the first active region, on a surface of the second silicon oxide film and etching a part of the second silicon oxide film existing on the main surface of the first active region, forming a first gate oxide film on the main surface of the first active region, removing the first mask, forming a second mask, having openings on a main surface of the second active region and etching a part of the second silicon oxide film existing on the main surface of the second active region, removing the second mask, forming a second gate oxide film on the main surfaces of the first and second active regions, and forming first field effect transistors and second field effect transistors on the main surfaces of the first and second active regions, wherein even though the silicon oxide films having different film thicknesses are formed on surfaces of a plurality of active regions in a single chip, the silicon oxide films in the grooves are not dropped along edges of the grooves; and therefore shapes of portions of the active regions in contact with trench isolation can be

formed substantially the same and transistor properties are not affected by the shapes of the active regions.

According to a fifth aspect of the present invention, there is provided a method of manufacturing a semiconductor device, wherein: the first mask is made of a polycrystalline film, whereby the silicon oxide films can be further controllably etched because a selectivity of 50 or more of the polycrystalline film is assured when the silicon oxide films are dry-etched.

According to a sixth aspect of the present invention, there is provided a method of manufacturing a semiconductor device, further comprising steps of: forming an inter-layer insulating film having openings on the inter-layer insulating film, which can reach the first field effect transistors, and forming capacitors which can reach the first field effect transistors through the openings, wherein leakage currents are restricted by making the gate oxide film of the DRAM memory cell thick; it becomes possible to make the shapes of the active region, which drop along the edges of the grooves even though driving capabilities are increased by making the gate oxide film of the other regions thin; and therefore a decrement of a threshold voltage can be restricted by suppressing an inverse narrow channel effect.

According to a seventh aspect of the present invention, there is provided a method of manufacturing a

semiconductor device, further comprising steps of: injecting channels of the first field effect transistors in the first active region before etching the second silicon oxide film on the main surface of the first active region after forming the first mask, and injecting channels of the second field effect transistors in the second active region before etching the second silicon oxide film on the main surface of the second active region after forming the second mask, wherein the channels are injected through the second silicon oxide film; the second silicon oxide film is removed; and the gate oxide film is again formed, whereby it becomes possible to obtain the gate oxide film having an excellent film quality by protecting the surface of the semiconductor substrate at the time of injecting channels.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete application of the invention and many of the attendant advantages thereof will be readily obtained as the same becomes better understood by reference to the following detailed description when considered in connection with the accompanied drawings, wherein:

Figure 1 is a cross-sectional view for schematically showing a part of a semiconductor device according to Embodiment 1 of the present invention;

Figure 2 is a cross-sectional view for schematically

showing a part of the semiconductor device according to Embodiment 1 of the present invention;

Figure 3 is a cross-sectional view for schematically illustrating the semiconductor device according to Embodiment 1 in a step of a method of manufacturing the semiconductor device;

Figure 4 is a cross-sectional view for schematically illustrating the semiconductor device according to Embodiment 1 in a step of a method of manufacturing the semiconductor device;

Figure 5 is a cross-sectional view for schematically illustrating the semiconductor device according to Embodiment 1 in a step of the method of manufacturing the semiconductor device;

Figure 6 is a cross-sectional view for schematically illustrating the semiconductor device according to Embodiment 1 in a step of the method of manufacturing the semiconductor device;

Figure 7 is a cross-sectional view for schematically illustrating the semiconductor device according to Embodiment 1 in a step of the method of manufacturing the semiconductor device;

Figure 8 is a cross-sectional view for schematically illustrating the semiconductor device according to Embodiment 1 in a step of the method of manufacturing the semiconductor device;

Figure 9 is a cross-sectional view for schematically

illustrating the semiconductor device according to Embodiment 1 in a step of the method of manufacturing the semiconductor device;

Figure 10 is a cross-sectional view for schematically illustrating the semiconductor device according to Embodiment 1 in a step of the method of manufacturing the semiconductor device;

Figure 11 is a cross-sectional view for schematically illustrating the semiconductor device according to Embodiment 1 in a step of the method of manufacturing the semiconductor device;

Figure 12 is a cross-sectional view for schematically illustrating the semiconductor device according to Embodiment 1 in a step of the method of manufacturing the semiconductor device;

Figure 13 is a cross-sectional view for schematically illustrating the semiconductor device according to Embodiment 1 in a step of the method of manufacturing the semiconductor device;

Figure 14 is a cross-sectional view for schematically illustrating the semiconductor device according to Embodiment 1 in a step of the method of manufacturing the semiconductor device;

Figure 15 is a cross-sectional view for schematically illustrating the semiconductor device according to Embodiment 1 in a step of the method of manufacturing the semiconductor device;

Figure 16 is a cross-sectional view for schematically illustrating a semiconductor device according to Embodiment 2 in a step of a method of manufacturing the semiconductor device;

Figure 17 is a cross-sectional view for schematically illustrating the semiconductor device according to Embodiment 2 in a step of the method of manufacturing the semiconductor device;

Figure 18 is a cross-sectional view for schematically illustrating the semiconductor device according to Embodiment 2 in a step of the method of manufacturing the semiconductor device;

Figure 19 is a cross-sectional view for schematically illustrating the semiconductor device according to Embodiment 2 in a step of the method of manufacturing the semiconductor device;

Figure 20 is a cross-sectional view for schematically showing a part of a conventional semiconductor device;

Figure 21 is a cross-sectional view for schematically showing a part of the conventional semiconductor device;

Figure 22 is a cross-sectional view of a conventional semiconductor device for illustrating a step of a method of producing the device;

Figure 23 is a cross-sectional view of the conventional semiconductor device for illustrating a step

of the method of manufacturing the device;

Figure 24 is a cross-sectional view of the conventional semiconductor device for illustrating a step of the method of manufacturing the device;

Figure 25 is a cross-sectional view of the conventional semiconductor device for illustrating a step of the method of manufacturing the device;

Figure 26 is a cross-sectional view of the conventional semiconductor device for illustrating a step of the method of manufacturing the device; and

Figure 27 is a cross-sectional view of the conventional semiconductor device for illustrating a step of the method of manufacturing the device.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A detailed explanation will be given of preferred embodiments of the present invention in reference to Figures 1 through 27 as follows, wherein the same references are used for the same or the similar portions and description of these portions is omitted.

EMBODIMENT 1

Figures 1 and 2 are cross-sectional views of a semiconductor device according to Embodiment 1 of the present invention, wherein Figure 2 is a cross-sectional view taken along a line A-A of Figure 1. In Figure 1, numerical reference 1 designates a semiconductor substrate; numerical reference 2 designates a groove; numerical references 3 and 4 designate silicon oxide

films; numerical references 51 and 52 designate gate oxide films; numerical reference 6 designates a polycrystalline layer; numerical reference 7 designates a metallic silicide layer; numerical reference 8 designates a side wall; numerical reference 9 designates a gate electrode; numerical references 10 through 15 designate source/drain areas; numerical references 61 and 62 designate inter-layer insulating films; numerical references 16 and 23 designate contact holes; numerical reference 17 designates a wire; numerical reference 18 designates a storage node; numerical reference 19 designates a capacitor insulating film; numerical reference 20 designates a cell plate; and numerical reference 22 designates a capacitor. The gate electrode 9 is composed of the polycrystalline layer 6 and the metallic silicide layer 7 such as tungsten silicide, wherein trench isolation is composed of the groove 2, the silicon oxide film 3, and the silicon oxide film 4. The capacitor 22 is composed of the storage node 18 made of polycrystalline silicon containing phosphorus of about 1 through 5 $\times$ $10^{20}/cm^3$, the capacitor insulating film 19 made of silicon oxinitride film having a film thickness of about 5 through 10 nm, and the cell plate 20 made of polycrystalline silicon containing phosphorus of about 1 through 5 $\times$ $10^{20}/cm^3$. The trench isolation is composed of the groove 2, the silicon oxide film 3, and the silicon oxide film 4, which trench isolation separate active

regions.

The wire 17 is connected to the source/drain area 12 through the contact hole 16, and the capacitor 22 is connected to the source/drain area 11 through the contact hole 23. Wires for respectively connecting to the source/drain areas 10 and 13, and the gate electrodes 9 through contact holes, formed in the inter-layer insulating film, are formed (not shown).

In Figure 1, when for example the gate length L_2 of the transistor in the logic circuit as the second field effect transistor is about 200 nm, the width of the groove 2 in the logic circuit is about 200 nm through 500 nm and the depth is about 150 through 500 nm. However, the width of the groove 2 is not unique and may become about 5,000 nm, in such a case by, for example, the semiconductor substrate 1 is left as a dummy pattern in portions without forming the element to adjust the width of the groove 2, whereby an evenness of a surface of the silicon oxide film 4 after embedding can be made small.

The silicon oxide film 3 of about 5 through 30 nm is formed to cover the surface of the semiconductor substrate in the groove 2, and the inside of the groove 2 is embedded by the silicon oxide film 4. On the surface of the semiconductor substrate 1 in the active region of the logic circuit, a gate oxide film 52 of about 4 through 7 nm is formed. The polycrystalline layer 6 of about 50 through 150 nm and the gate electrode 9 made of

the metallic silicide layer 7 having a film thickness of about 50 through 150 nm are formed thereon. In a case that influences of defects in the semiconductor substrate 1 to element properties are sufficiently small, the silicon oxide film 3 can be omitted.

The polycrystalline layer 6 contains phosphorus and arsenic of about $1 \times 10^{21}/cm^3$ in nMOS or boron, boron fluoride and so on of about $1 \times 10^{21}/cm^3$ in pMOS. On the other hand, the source/drain areas 12 and 13 contain phosphorus and arsenic, or boron, boron fluoride and so on respectively of about $1 \times 10^{18}/cm^3$, wherein the source/drain areas is in a lightly doped drain (LDD) structure having a region containing arsenic of about $1 \times 10^{20}/cm^3$ when necessary.

When, for example, the gate length L_1 of the transistor of the DRAM memory cell as the first field effect transistor is about 200 nm, the widths of the grooves 2 is not the same with respect to their locations such that the minimum width is 100 nm through 200 nm and the ordinary width is about 200 nm through 400 nm, and the depths of the grooves 2 are about 150 through 500 nm. Incidentally, the film thicknesses of the gate oxide films are about 7 through 10 nm. Portions not described in the above have a structure similar to that in the logic circuit.

In the DRAM memory cell, information is accumulated by means of electric charges stored in the capacitors;

and a refleshing including reading and writing is conducted at a predetermined period, wherein when leakage currents flow, the information stored in the capacitors is excessively lost to deteriorate a refresh property. Therefore, restriction of leakage currents is important in comparison with transistors in the other portions.

When data are written in the capacitor 22, voltages are applied to electrodes of the memory cell such as V_G=2.0V and V_B=-1.0V, and simultaneously 0V is applied to a bit line (not shown) connected to the source/drain area 10. On the other hand, when data are erased, V_G=2.0V, V_B=-1.0V, and a bit line (not shown) connected to the source/drain area 10 is applied with a voltage of about 2.0V. When the data are read out, a voltage applied to the bit line is about 1.0V.

In the logic circuit, by applying voltages to the gate electrode 9, the source/drain areas 12, 13, and semiconductor substrate 1 (well), a channel is formed in a surface of the semiconductor substrate 1 under the gate electrode 9, wherein one of the source/drain areas 12, 13 is a source and the other is a drain, whereby the logic circuit works as a circuit. When an nMOS transistor is used, voltages to be applied to electrodes of the logic circuit are respectively V_G=2.5V, V_D=2.5V, V_S=0V, and V_B=0V, where references V_G, V_D, V_S, and V_B respectively designate a voltage respectively applied to a gate, a drain, a source, and a semiconductor substrate.

In Embodiment 1, a semiconductor device, in which portions other than the DRAM memory cell has two transistors in these active regions, is used for explanation. However, the present invention is not limited thereto.

According to this semiconductor device, despite formation of a plurality of gate oxide films having different film thicknesses in a single chip, a part of the silicon oxide film 4 along edges of the grooves 2 are not dropped, and shapes of ends of active regions, in contact with trench isolation, can be formed substantially the same, whereby transistor properties are not affected by the shapes of the active regions. Therefore, it is possible to form DRAM having a good refresh property with a small consumption power and high reliability obtained by restriction of a leakage current using a thick gate oxide film and form a logic circuit having a high driving capability using a thin gate oxide film, being a high speed, and having high reliability obtained by restriction of a drop of a threshold voltage as a result of suppression of an inverse narrow channel effect, both in a single chip, whereby miniaturization of the chip is attained maintaining good properties of the semiconductor device.

Further, at portions where the widths of the grooves 2 surrounding these active regions are the same, there is no scattering in the heights of the surfaces of the

silicon oxide films 4 between a position adjacent to an active region formed with the thick gate oxide film 51 and a position adjacent to the active region formed with the thin gate oxide film 52. Thus, it becomes possible to maintain a margin of a depth of focus in a photolithographing process at a time of patterning a gate electrode, and a short does not occur by a remaining gate electrode material left at a time of etching a gate electrode material deposited on the surfaces of the silicon oxide film 4. On the other hand, the surface of the semiconductor substrate is not shaved by excessively etching in order to completely remove the gate electrode material and penetrating the gate oxide film as an etching stopper. Therefore, reliability of the semiconductor device is improved without an incident that leakage currents flow through surface roughness of the semiconductor substrate.

Figures 3 through 14 are cross-sectional views for illustrating steps of a method of manufacturing the semiconductor device according to Embodiment 1 of the present invention. As shown in Figures 8 through 14, a portion in which a thick gate oxide film is formed (hereinbelow, referred to as a thick film portion) and a portion in which thin gate oxide film is formed (hereinbelow, referred to as a thin film portion) are adjacent each other. Hereinbelow, an example that the DRAM memory cell and a sense amplifier are formed in the

thick film portion and the logic circuit is formed in the thin film portion is shown. In Figure 3, numerical reference 21 designates a silicon nitride film; and numerical reference 31 designates a silicon oxide film.

After forming the silicon oxide film 31 having a thickness of about 5 through 30 nm on the semiconductor substrate 1 by thermal oxidation, the silicon nitride film of about 100 through 300 nm is formed. Figure 3 is a cross-sectional view of the semiconductor device after this step.

In the next, anisotropic etching is conducted using a photolithographing pattern (not shown) such as a photoresist formed in portions other than areas for receiving grooves 2. The photolithographing pattern is removed after patterning the silicon nitride film 2. Figure 4 is a cross-sectional view of the semiconductor device after this step.

The silicon oxide film 31 and the semiconductor substrate 1 are subject to anisotropic etching using the remaining silicon nitride film 21 as a mask to form the groove 2 having a depth of 100 through 500 nm on the surface of the semiconductor substrate 1 and the groove 2 having a width of about 100 through 500 nm in the logic circuit. At this time, the width of the groove 2 in the DRAM memory cell is about 100 nm through 200 nm at a portion having the minimum width of isolation and about 200 through 400 nm at portions other than this. Figure 5

is a cross-sectional view for illustrating elements of the semiconductor device after this step.

In the next, the silicon oxide film 4 having a thickness of about 300 nm through 1,000 nm is formed on a whole surface by a low-pressure CVD method; and the silicon oxide film 4 on a surface of the silicon nitride film 21 is removed by a chemical mechanical polishing (CMP) method using the silicon nitride film 21 as a stopper to thereby remain the silicon oxide film 4 only in insides of the openings fabricated by the grooves 2 and the silicon nitride film 21. After removing the silicon nitride film 21 by a wet etching using thermal phosphoric acid, the silicon oxide film 31 is removed. Figure 6 illustrates a cross-sectional view after this step.

In Figure 7, numerical reference 32 designates a silicon oxide film. In the silicon oxide film 32 of about 3 through 15 nm is formed on a surface of the semiconductor substrate 1 by thermal oxidation. Figure 7 is a cross-sectional view for illustrating elements of the semiconductor device after this step. In a case of nMOS, ions such as boron or boron fluoride are implanted over a mask having openings corresponding to nMOS; and in a case of pMOS, ions of impurities such as phosphorus or arsenic are implanted over a mask having openings corresponding to pMOS, wells (not shown) other than channel implantation layers are formed in the DRAM memory

cell and portions other than the DRAM memory cell. This ion-implanting for forming wells can be simultaneously conducted at a time of forming the channel implantation layers, if necessary.

In Figure 8, numerical reference 211 designates a silicon nitride film; and numerical reference 41 designates a resist pattern. After forming the silicon nitride film 211 of about 5 through 30 nm is formed on the silicon oxide film 32, the resist pattern having openings of active regions of the thick-film memory cell, and the silicon nitride film 211 on the surface of the semiconductor substrate 1 of the memory cell is removed using this resist pattern 41. Thereafter, the channel implantation layers (not shown) of the memory cell is formed by implanting ions of boron or boron fluoride. Figure 8 is a cross-sectional view for illustrating the semiconductor device after this step.

In Figure 9, numerical reference 42 designates a resist pattern. The resist pattern 41 is removed; the resist pattern 42 having openings of the active regions of the sense amplifier, which uses transistors having a different threshold voltage from that in the memory cell, is formed in the thick film portion; and the silicon nitride film 211 formed on a surface of the semiconductor substrate 1 of the sense amplifier is removed. Thereafter, a channel implantation layer (not shown) is formed in the active region of the sense amplifier by

implanting ions such as boron. Figure 9 is a cross-sectional view of the semiconductor device after this step. In the thick film portion, when transistors having a further different threshold voltage exist, formation of the resist pattern and implantation of ions may be repeatedly conducted in a similar manner.

In Figure 10, numerical reference 53 designates a silicon oxide film. After removing the resist pattern 42 and the silicon oxide film 32 in the thick film portion by hydrofluoric acid using the silicon nitride film 211 as a mask, thermal oxidation is conducted again to thereby form the gate oxide film 53. Figure 10 is a cross-sectional view of the semiconductor device after this step, in which the gate oxide film 53 is formed in the memory cell and the sense amplifier within a surface of the semiconductor substrate 1, and the silicon oxide film 32 and the silicon nitride film 211 are formed in the logic circuit.

In Figure 11, numerical reference 43 designates a resist pattern. After removing the silicon nitride film 211, the active regions of pMOS of the thick film portion and the thin film portion are covered, and an impurity such as boron and boron fluoride is injected as an ion using a mask of the resist pattern 43, in which the active region of nMOS of the thin film portion is opened, whereby a channel implantation layer (not shown) of nMOS of the logic circuit is formed. In a case of pMOS, in a

manner similar to that in nMOS, the active regions of nMOS of the thick film portion and the thin film portion are covered to form a channel implantation layer (not shown) by injecting ions such as phosphorus and arsenic using a mask, in which the active region of pMOS of the thin film portion is opened. Thereafter, the silicon oxide film 32 is removed. Figure 11 is a cross-sectional view for illustrating the semiconductor device after this step. Although description is made for a case that the threshold voltages of nMOS and pMOS in the logic circuit are respectively one kind, it is necessary to repeatedly inject a channel by separately masking depending on conduction types of channel implantation layers and threshold voltages.

After removing the resist pattern 43, the silicon oxide film 52 having a film thickness of about 4 through 7 nm is formed on a whole surface by thermal oxidation. Figure 12 is a cross-sectional view of the semiconductor device after this step. At this stage, the channel implantation layers are formed in transistors in all areas of the DRAM memory cell, the sense amplifier, and the logic circuit. In Embodiment 1, although the sense amplifier is formed in the thick film portion, it may be formed in the thin film portion. The ions are simultaneously implanted in portions having the same gate oxide film thickness, the same conduction types of the channel implantation layers, and the concentration of

impurities in the channel implantation layers.

In the next, after depositing the polycrystalline layer 6, which contains impurities of about $1 \times 10^{21}/cm^3$, such as phosphorus and arsenic in a case of nMOS, and boron and boron fluoride in a case of pMOS and has a film thickness of about 50 through 100 nm, by a CVD method and forming a metal silicide layer 7 such as tungsten silicide by a CVD method or a sputtering method, a gate electrode 9 is formed by patterning.

Source/drain areas 10 through 15 are formed by injecting ions of about $3 \times 10^{13}/cm^2$ of phosphorus or arsenic in nMOS or of boron or boron fluoride in pMOS under about 20 through 40 keV; and side walls 8 are formed by depositing and etching-back the silicon oxide film by about 50 through 100 nm using a low pressure CVD method. Figure 13 is a cross-sectional view for illustrating the semiconductor device after this step. When the source/drain areas 12 through 15 are made to be a lightly doped drain (LDD) structure, portions receiving the memory cell is covered by a mask, and the source/drain areas (not shown) include impurity regions having a concentration of impurities of about $1 \times 10^{20}/cm^3$ formed by implanting arsenic in nMOS or boron or boron fluoride in pMOS.

Thereafter, an inter-layer insulating film 61 of about 200 through 600 nm is deposited by a low-pressure CVD method, and a contact hole 16 reachable the

source/drain area 12 is opened to have a diameter between 0.1 μm through 0.5 μm by a dry etching method. After depositing a polycrystalline silicon of about 50 through 150 nm containing phosphorus of about 1×10^{20} through $5 \times 10^{20}/cm^3$ by a CVD method, tungsten silicide (WSi) of 50 through 150 nm is deposited by a CVD method and patterned to form a wire 17. Figure 14 is a cross-sectional view for illustrating the semiconductor device after this step.

Further, after forming an inter-layer insulating film (not shown), contact holes (not shown) are formed; and a wire material is embedded in the contact holes, whereby a wire connected to the source/drain area 10 (bit line) and wires connected to the source/drain areas 13 through 15 are formed (not shown). Wires connected to the source/drain areas 10, and 12 through 15 can be formed in any order for the convenience of a circuit structure.

After forming an inter-layer insulating film 62 and a contact hole 23, polycrystalline silicon of about 600 through 1,000 nm containing an impurity such as phosphorus of about 1×10^{20} through $5 \times 10^{20}/cm^3$ is deposited on a whole surface and is arranged at a predetermined area by patterning, whereby a storage node 18 is formed. Thereafter, by depositing a silicon oxynitride film of about 5 through 10 nm, to be a capacitor insulating film 19, is deposited by a CVD method, and by depositing and patterning polycrystalline

silicon of about 50 through 100 nm containing an impurity such as phosphorus of about 1×10^{20} through $5 \times 10^{20}/cm^3$, to be a cell plate 20, a capacitor 22 is formed. As described, the semiconductor device shown in Figure 1 is formed.

Further, at the step that the contact holes reachable to the source/drain areas 10 through 15 are formed, areas of impurities having the same conduction types as the source/drain areas exposed to the contact holes can be formed by injecting self aligned contact (SAC). Such areas of impurities are formed by injecting phosphorus of 1×10^{13} through $1 \times 10^{14}/cm^2$ under 50 through 150 keV so as to have a concentration of impurities of about $1 \times 10^{18}/cm^3$, whereby it becomes possible to relax an electric field of a p-n junction caused by a peak of a concentration of impurities between the channel implantation layer and the source/drain areas and to restrict leakage currents from the capacitor 22 to the semiconductor substrate 1 (well), whereby a refresh property becomes satisfactory and reliability of the semiconductor device is improved. Further, in portions other than memory cell, by injecting ions of about 5×10^{13} through $30 \times 10^{13}/cm^2$, i.e. phosphorus in nMOS, and boron or boron fluoride in pMOS, under 20 through 50 keV to make areas of impurity having a concentration of impurities of about $5 \times 10^{18}/cm^3$, it becomes possible to

reduce contact resistances between wires embedded in the contact holes and the source/drain areas; and a driving capability is improved.

Although, in Embodiment 1, the semiconductor device in which the logic circuit, the DRAM memory cell, and the sense amplifier are formed, is described, the present invention is not specifically limited thereto as long as a plurality of thicknesses of gate oxide films are used in a single chip.

In accordance with the method of manufacturing this semiconductor device, since the number and the conditions for removing the silicon oxide films formed on the surface of the active region are substantially equal in the step of forming the plurality of gate oxide films having different film thicknesses in the single chip, the portion of the silicon oxide film 4 along the edge of the groove 2 is not dropped. Accordingly, even though the gate oxide films having different film thicknesses are formed on the surface, it becomes possible to form the portion of the active region in contact with the trench isolation substantially the same, and the properties of the transistor are not affected by the shape of the active region. Therefore, transistor properties are not affected by the shapes of the active region. Thus, it is possible to obtain the method of manufacturing the semiconductor device miniaturized maintaining the desirable semiconductor device properties, in which the

DRAM memory cell with improved refresh characteristics, a low consumption power, and improved reliability by restricting leakage currents using the thick gate oxide film and the logic circuit with an improved driving capability, a high speed, and improved reliability which can restrict a drop of the threshold voltage by suppressing an inverse narrow channel effect using the thin gate oxide film.

Further, since the number and the conditions for etching the surfaces of the silicon oxide film 4 are the same in both of the portion adjacent to the active region having the thick gate oxide film and the portion adjacent to the active region having the thin gate oxide film, there is no scattering in the heights of the surfaces of the silicon oxide films 4 in grooves 2 having the same widths. Thus, it is possible to assure a margin with respect to a depth of focus in the photolithographing process at the time of patterning the gate electrode, and a short caused by the gate electrode material remained at a time of etching the material deposited on the surfaces of the silicon oxide films 4 does not occur. On the other hand, since the surface of the semiconductor substrate is not shaved as long as an excessive etching for completely remove the gate electrode material is not conducted and the gate oxide film having an etching stopper is not penetrated, an yield is improved, and reliability is improved without a danger of generating

leakage currents caused by a rough surface of the semiconductor substrate.

In Figure 15, numerical reference 212 designates a polycrystalline film. After forming the trench isolation on the surface of the semiconductor substrate, the silicon oxide film 32 is formed on the surface; and the polycrystalline film 212 is formed thereon. Figure 15 is a cross-sectional view for illustrating the semiconductor device at this stage. The polycrystalline film 212 is formed instead of the silicon nitride film 211 as a mask for etching the silicon oxide film 32. The order of removing the silicon oxide film 32 using a plurality of resist patterns is similar to that in the silicon nitride film 211. Removal of this polycrystalline film is conducted by an isotropic dry etching. Although the selectivity of the silicon nitride film is about 3 through 20 at a time of dry-etching the silicon oxide film 32, because the selectivity of the polycrystalline film is assured to be 50 or more, it is possible to controllably etch the silicon oxide film 32 and it is effective for microminiaturizing the semiconductor device.

EMBODIMENT 2

Figures 16 through 18 are cross-sectional views for illustrating steps of the method of manufacturing the semiconductor device according to Embodiment 2 of the present invention, wherein Embodiment 2 is another method of manufacturing the semiconductor device described in

Embodiment 1. According to the method of manufacturing, the semiconductor device shown in Figure 1 can be manufactured.

In a similar manner to Embodiment 1, trench isolation composed of a groove 2 and silicon oxide films 3 and 4 is formed on a surface of a semiconductor substrate. A silicon oxide film 32 is formed in a similar manner to Embodiment 1; boron or boron fluoride are implanted as an ion after forming a mask, in which a portion corresponding to nMOS is opened; and an impurity such as phosphorus or arsenic is implanted as an ion after forming a mask, in which a portion corresponding to pMOS is opened, to thereby form a well (not shown) other than channel implantation layer in a memory cell and portions other than this. These steps are the same as those in Embodiment 1.

In Figure 16, numerical reference 44 designates a resist pattern. After forming a silicon nitride film 211 of 5 through 30 nm on the silicon oxide film 32 in a similar manner to Embodiment 1, a resist pattern 44 for covering a thin film portion is formed, and the silicon nitride film 211 on the surface of the semiconductor substrate 1 in a thick film portion is removed using this resist pattern 44. Figure 16 is a cross-sectional view for illustrating the semiconductor device after this step. Even though, in Embodiment 1, the channel implantation layer is formed and the silicon nitride film 211 is

simultaneously removed with respect to portions having different threshold voltages such as the memory cell and the sense amplifier when the portions have the same thicknesses of gate oxide films, the silicon nitride film 211 is removed with respect to portions having the same thicknesses of the gate oxide films.

In the next, after removing the resist pattern 44, a resist pattern 41, in which an active region of the memory cell is opened, is formed, and a channel implantation layer (not shown) of the memory cell is formed by implanting boron or boron fluoride as an ion. Figure 17 is a cross-sectional view of the semiconductor device after this step.

After removing the resist pattern 41, a resist pattern 42, in which an active region of the sense amplifier is opened, is formed, and the channel implantation layer (not shown) of the sense amplifier is formed by implanting ions. Figure 18 is a cross-sectional view for illustrating the semiconductor device after this step. Similarly to Embodiment 1, when transistors having further different threshold voltages exist in the thick film portion, formation of a resist pattern and ion-implantation are similarly repeated.

In the next, in a similar manner to Embodiment 1, after removing the resist pattern 42, the silicon oxide film 32 on the surface of the semiconductor substrate in the thick film portion is removed using the silicon

nitride film 211 as a mask and thereafter a silicon oxide film 53 is again formed by thermal oxidation. After removing the silicon oxide film 32 remaining in the surface of the semiconductor substrate in the logic circuit in a similar manner to Embodiment 1, the silicon oxide film 52 having a film thickness of about 4 through 7 nm is formed on a whole surface by thermal oxidation. Similarly to Embodiment 1, a gate electrode 9, source/drain areas 10 through 13, a side wall 8, an inter-layer insulating film 61, a wire 17, an inter-layer insulating film 62 and a capacitor 22 are formed. As described, the semiconductor device shown in Figure 1 is formed.

According to a method of manufacturing the semiconductor device of the present invention, because the number and the conditions of removing the silicon oxide film formed on these surfaces of the active regions are made substantially the same in the step of forming the plurality of gate oxide films having different thicknesses in the single chip, the portions of the silicon oxide film 4 along the edge of the grooves 2 are not dropped. Accordingly, even though the gate oxide films having different thicknesses are formed on the surface, it is possible to make shapes of portions of the active regions in contact with the trench isolation substantially the same, whereby transistor properties are not affected by the shapes of the active regions. Thus,

it is possible to form a DRAM memory cell having improved refresh properties, a low consumption power, and improved reliability by suppressing leakage currents using the thick gate oxide film and a logic circuit, in which a driving capability is improved, a drop of the threshold voltage can be restricted by suppressing an inverse narrow channel effect, a high speed and improved reliability are obtainable using the thin gate oxide film, in the single chip, whereby the method of manufacturing the semiconductor device miniaturized maintaining desirable properties of the device is obtainable.

Further, since the number and the conditions of etching the surface of the silicon oxide film 4 is the same with respect to portions adjacent to active regions having the thick gate oxide film and portions adjacent to active regions having the thin gate oxide film, the heights of the surfaces of the silicon oxide films 4 are not scattered as long as the widths of the grooves 2 are equal. Thus, it is possible to assure a margin of a depth of focus in a photolithographing process at a time of patterning the gate electrode, a short, caused by a gate electrode material remaining at a time of etching the gate electrode material deposited on the surface of the silicon oxide film 4, does not occur. On the other hand, the surface of the semiconductor substrate is not shaved because an etching for completely removing the gate electrode material is not excessively conducted and

the gate oxide film as an etching stopper is not penetrated, whereby an yield is improved; and there is no danger that leakage currents are generated by surface roughness of the semiconductor substrate, wherein the semiconductor device having improved reliability is obtainable.

Further, according to the method of manufacturing the semiconductor device described in Embodiment 1, it may occur that an end portion of the silicon nitride film 211 is covered above the trench isolation located between the sense amplifier and the memory cell at a time of forming the resist pattern 42 having openings above the sense amplifier as shown in Figure 19; and the silicon nitride film 211 is left without being etched in the end portion. When the silicon nitride film 211 is left, the silicon oxide film 32 therebelow is not etched; and the gate oxide film 53 is not formed by thermal oxidation, whereby the silicon oxide film 32 is left as a gate oxide film at this part. In this case, a dielectric breakdown of the gate oxide film may occur because a quality of film is deteriorated after various steps such as ion-implanting for forming a well. On the contrary, according to the method of manufacturing the semiconductor device described in Embodiment 2, when the silicon nitride film 211 used as a mask for determining the thicknesses of the gate oxide films 51 and 52 is removed after removing the whole silicon nitride film 211

in the thick film portion by the resist pattern 44, requisite treatment such as channel implantation is conducted; and the remaining silicon nitride film 211 is selectively removed by hot phosphoric acid or the like. By such a method, because the silicon nitride film 211 is not left by a deviation of the resist pattern, an yield is improved by maintaining a margin of the resist pattern.

Similarly to Embodiment 1, when the polycrystalline film is used instead of the silicon nitride film 211, because the selectivity of the polycrystalline film is higher than that of the silicon nitride film in dry-etching the silicon oxide film 32, it is possible to more controllably etch the silicon oxide film 32, whereby microminiaturization of the semiconductor device can be effectively conducted.

The first advantage of a semiconductor device according to the present invention is that miniaturization of a chip is attainable keeping properties of elements respectively formed in a thick film portion and a thin film portion of gate oxide films desirable.

The second advantage of the semiconductor device according to the present invention is that a short caused by a remaining gate electrode material at a time of etching the material deposited on a surface of a silicon oxide film does not occur, and reliability of the device is improved without a danger of generating leakage

currents caused by surface roughness of a semiconductor substrate.

The third advantage of the semiconductor device according to the present invention is that miniaturization of a chip is attainable by maintaining properties of the semiconductor device desirable.

The forth advantage of a method of manufacturing the semiconductor device according to the present invention is that the semiconductor device having a miniaturized chip is obtainable maintaining properties of elements respectively formed in the thick film portion and the thin film portion of the gate oxide films desirable.

The fifth advantage of the method of manufacturing the semiconductor device according to the present invention is that the microminiaturizing semiconductor device is obtainable using a polycrystalline film as a mask for etching a second silicon oxide film.

The sixth advantage of the method of manufacturing the semiconductor device according to the present invention is that the miniaturized semiconductor device is obtainable while maintaining properties of the semiconductor device desirable.

The seventh advantage of the method of producing the semiconductor device according to the present invention is that the semiconductor device having high reliability is obtainable by protecting a surface of the semiconductor substrate by injecting channels of the

elements through the second silicon oxide film.

Obviously, numerous modifications and variations of the present invention are possible in light of the above teachings. It is therefore to be understood that within the scope of the appended claims, the invention may be practiced otherwise than as specifically described herein.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

grooves formed on a main surface of a semiconductor substrate,

silicone oxide films embedded in insides of said grooves,

a first active region surrounded by said grooves and disposed on a first part of said main surface of said semiconductor substrate,

a first field effect transistor having a first gate oxide film formed on a main surface of said first active region,

a second active region surrounded by said grooves and disposed on a second part on said main surface of said semiconductor substrate, and

a second field effect transistor having a second gate oxide film, having a thickness different from that of said first gate oxide film, formed on a main surface on said second active region, wherein

an end shape of said second active region is the same as that of said first active region.

2. The semiconductor device according to Claim 1, wherein

the widths of said grooves surrounding said first active region and said second active region are equal; and

the heights of these grooves from bottom surfaces to

surfaces of said silicon oxide films are equal.

3. The semiconductor device according to Claim 1 further comprising:

an inter-layer insulating film formed on a surface of said first field effect transistor and having an opening reachable to said first field effect transistor, and

a capacitor connected to said first field effect transistor through said opening, wherein

the thickness of the first gate oxide film is larger than the thickness of said second gate oxide film.

4. The semiconductor device according to Claim 2 further comprising:

an inter-layer insulating film formed on a surface of said first field effect transistor and having an opening reachable to said first field effect transistor, and

a capacitor connected to said first field effect transistor through said opening, wherein

the thickness of the first gate oxide film is larger than the thickness of said second gate oxide film.

5. A method of manufacturing a semiconductor device comprising steps of:

forming grooves surrounding first and second active regions disposed on a main surface of a semiconductor substrate,

forming a first silicon oxide film embedded in said

grooves,

forming a second silicon oxide film covering said first and second active regions,

forming a first mask having an opening corresponding to said first active region on a surface of said second silicon oxide film and etching said second silicon oxide film,

forming a first gate oxide film on said main surface of said first active region,

removing said first mask,

forming a second mask having an opening corresponding to said second active region and etching said second silicon oxide film,

removing said second mask,

forming a second gate oxide film on main surfaces of said first and second active regions, and

forming a first field effect transistor and a second field effect transistor respectively on said main surfaces of said first and second active regions.

6. The method of manufacturing the semiconductor device according to Claim 5, wherein

said first mask is a polycrystalline film.

7. The method of manufacturing the semiconductor device according to Claim 5, further comprising steps of:

forming an inter-layer insulating film,

forming an opening in said inter-layer insulating film reachable to said first field effect transistor,

forming a capacitor reachable to said first field effect transistor through said opening.

8. The method of manufacturing the semiconductor device according to Claim 6, further comprising steps of:

forming an inter-layer insulating film,

forming an opening in said inter-layer insulating film reachable to said first field effect transistor,

forming a capacitor reachable to said first field effect transistor through said opening.

9. The method of manufacturing the semiconductor device according to Claim 7, further comprising steps of:

injecting a channel of said first field effect transistor into said first active region after forming said first mask and before etching said second silicon oxide film on said main surface of said first active region, and

injecting a channel of said second field effect transistor into said second active region after forming said second mask and before etching said second silicon oxide film on said main surface of said second active region.

10. The method of manufacturing the semiconductor device according to Claim 8, further comprising steps of:

injecting a channel of said first field effect transistor into said first active region after forming said first mask and before etching said second silicon oxide film on said main surface of said first active

ABSTRACT OF THE DISCLOSURE

A semiconductor device and a method of manufacturing the semiconductor device, which semiconductor device comprises grooves formed on a main surface of a semiconductor substrate, silicon oxide films embedded in insides of the grooves, a first active region surrounded by the grooves and disposed on a first portion of the main surface of the semiconductor substrate, a first field effect transistor having a first gate oxide film formed on a main surface of the first active region, a second active region surrounded by the grooves and disposed on a second part on the main surface of the semiconductor substrate, and a second field effect transistor having a second gate oxide film, having a thickness different from that of the first gate oxide film, formed on a main surface of the second active region, wherein end shapes of the first active region and second active region are the same, by which drops of the silicon oxide films in the grooves along edges of the grooves do not occur.

APPENDIX C

Dept.: PP/JF

OSMM&N File No. 217208US2 By: MJS/bj

Serial No. NEW APPLICATION

In the matter of the Application of: Haruo FURUTA, et al.

For: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREFOR

The following has been received in the U.S. Patent Office on the date stamped hereon:

- ■ 36 pp. Specification 13 Claims/Formal Drawings 18 Sheets and 2 Pages Application Data Sheet
- ■ Combined Declaration, Petition & Power of Attorney 3 pages
- ☐ List of Inventor Names and Addresses
- ■ Utility Patent Application Transmittal
- ☐ CPA
- ■ Request for Priority
- ■ Priority Doc (1)
- ■ Check for $780.00
- ■ Dep. Acct. Order Form
- ■ Fee Transmittal Form
- ■ Assignment/PTO 1595 pages: 3
- ☐ Letter to Official Draftsman
- ☐ Letter Requesting Approval of Drawing Changes
- ☐ Drawings sheets ☐ Formal
- ☐ Letter
- ☐ Amendment
- ■ Information Disclosure Statement
- ■ PTO-1449
- ■ Cited References (1)
- ☐ Search Report
- ☐ Statement of Relevancy
- ■ Cited Pending Applications (1)
- ■ IDS/Related/List of Related Cases
- ☐ Restriction Response
- ☐ Election Response
- ☐ Rule 132 Declaration
- ☐ Petition for Extension of Time
- ☐ Notice of Appeal
- ☐ Brief
- ☐ Issue Fee Transmittal
- ■ White Advance Serial Number Card
- ☐ Small Entity Status is claimed
- ☐
- ☐

OIPE JC177 DEC 14 2001 PATENT & TRADEMARK OFFICE

Due Date: 12/15/01

APPENDIX D

Docket No. 217208US2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Haruo FURUTA, et al.

SERIAL NO: NEW APPLICATION GAU:

FILED: HEREWITH EXAMINER:

FOR: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREFOR

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Applicant(s) wish to disclose the following information.

REFERENCES

☒ The applicant(s) wish to make of record the references listed on the attached form PTO-1449. Copies of the listed references are attached, where required, as are either statements of relevancy or any readily available English translations of pertinent portions of any non-English language references.

☐ A check is attached in the amount required under 37 CFR §1.17(p).

RELATED CASES

☒ Attached is a list of applicant's pending application(s) or issued patent(s) which may be related to the present application. A copy of the patent(s), together with a copy of the claims and drawings of the pending application(s) is attached along with PTO 1449.

☐ A check is attached in the amount required under 37 CFR §1.17(p).

CERTIFICATION

☐ Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.

☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

DEPOSIT ACCOUNT

☒ Please charge any additional fees for the papers being filed herewith and for which no check is enclosed herewith, or credit any overpayment to deposit account number 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Marvin J. Spivak

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(OSMMN 10/01)

LIST OF RELATED CASES

Docket Number	Serial or Patent No.	Filing or Issue Date	Status or Patentee
PER CLIENT	09/340,504	UNKNOWN	UNKNOWN

GJM/sb
I:\em\EMRel\217s218s\217208US LIST new appl.wpd

APPENDIX G

Docket No. 217208US2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTOR(S) Haruo FURUTA, et al.

SERIAL NO: New Application

FILING DATE: Herewith

FOR: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREFOR

FEE TRANSMITTAL

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

FOR	NUMBER FILED	NUMBER EXTRA	RATE	CALCULATIONS
TOTAL CLAIMS	13 - 20 =	0	× $18 =	$0.00
INDEPENDENT CLAIMS	3 - 3 =	0	× $84 =	$0.00
☐ MULTIPLE DEPENDENT CLAIMS (If applicable)			+ $280 =	$0.00
☐ LATE FILING OF DECLARATION			+ $130 =	$0.00
			BASIC FEE	$740.00
			TOTAL OF ABOVE CALCULATIONS	$740.00
☐ REDUCTION BY 50% FOR FILING BY SMALL ENTITY				$0.00
☐ FILING IN NON-ENGLISH LANGUAGE			+ $130 =	$0.00
☒ RECORDATION OF ASSIGNMENT			+ $40 =	$40.00
			TOTAL	$780.00

☐ Please charge Deposit Account No. 15-0030 in the amount of $0.00 A duplicate copy of this sheet is enclosed.

☒ A check in the amount of $780.00 to cover the filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge any additional fees which may be required for the papers being filed herewith and for which no check is enclosed herewith, or credit any overpayment to Deposit Account No. 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully Submitted,

OBLON, SPIVAK, McCLELLAND,
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APPENDIX F

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	217208US2
First Inventor or Application Identifier	Haruo FURUTA, et al.
Title	SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREFOR
Assignee Name:	MITSUBISHI DENKI KABUSHIKI KAISHA
Assignee Address:	2-3, Marunouchi 2-chome, Chiyoda-ku, Tokyo 100-8310 Japan

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents

1. ☒ Fee Transmittal Form (e.g. PTO/SB/17) (Submit an original and a duplicate for fee processing)
2. ☒ Specification — Total Sheets: 36
3. ☒ Formal Drawing(s) *(35 U.S.C. 113)* — Total Sheets: 18
4. ☒ Oath or Declaration — Total Pages: 3
   a. ☒ Newly executed (original)
   b. ☐ Copy from a prior application *(37 C.F.R. §1.63(d))* *(for continuation/divisional with box 17 completed)*
      i. ☐ DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see *37 C.F.R. §1.63(d)(2) and 1.33(b).*
5. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program *(Appendix)*
6. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. ☐ Computer Readable Form (CRF)
   b. Specification or Sequence Listing on :
      i. ☐ CD-ROM or CD-R (2 copies); or
      ii. ☐ Paper
   c. ☐ Statements verifying identity of above copies

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

ACCOMPANYING APPLICATION PARTS

7. ☒ Assignment Papers (cover sheet & document(s))
8. ☒ Application Data Sheet. See 37 CFR 1.76
9. ☐ 37 C.F.R. §3.73(b) Statement *(when there is an assignee)* ☐ Power of Attorney
10. ☐ English Translation Document *(if applicable)*
11. ☒ Information Disclosure Statement (IDS)/PTO-1449 ☒ Copies of IDS Citations (1)
12. ☐ Preliminary Amendment
13. ☒ White Advance Serial No. Postcard
14. ☒ Certified Copy of Priority Document(s) (1) *(if foreign priority is claimed)*
15. ☐ Applicant claims small entity status. *See 37 CFR 1.27*
16. ☒ Other: Request for Priority, Cited Pending Application (1), List of Related Cases

17. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below:*
☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application no.:
Prior application information: Examiner: Group Art Unit:

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

18. Amend the specification by inserting before the first line the sentence:
☐ This application is a ☐ Continuation ☐ Division ☐ Continuation-in-part (CIP)
of application Serial No. Filed on
☐ Which was published in English
☐ Which was not published in English
☐ This application claims priority of provisional application Serial No. Filed

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Signature:		Date:	12/14/01
Name:	C. Irvin McClelland Registration Number 21,124	Registration No.:	